

ABSTRACT

A chip packaging box

A chip packaging box, comprising a body, grid units provided on the body, and a positioning frame extending downwardly around an outer periphery of the body; a bottom surface of each of the grid units is provided with intersecting grooves; side walls of each of the grid units incline towards a center of the corresponding grid unit from top to bottom. The present invention is used for storage and transportation of chips. Identical grid units are provided on the surface of the present invention. Intersecting grooves are provided on the supporting surface that supports a chip at the bottom surface of each grid unit, such that the supporting surface of each grid unit does not entirely contact the bottom surface of the corresponding chip placed inside. Therefore, the influences of vacuum adherence and static electricity are reduced, thereby preventing the chip from adhering with its corresponding grid unit due to electrostatic adherence. Hence, the chip is being better protected.

Drawing accompanying the abstract: FIG. 3