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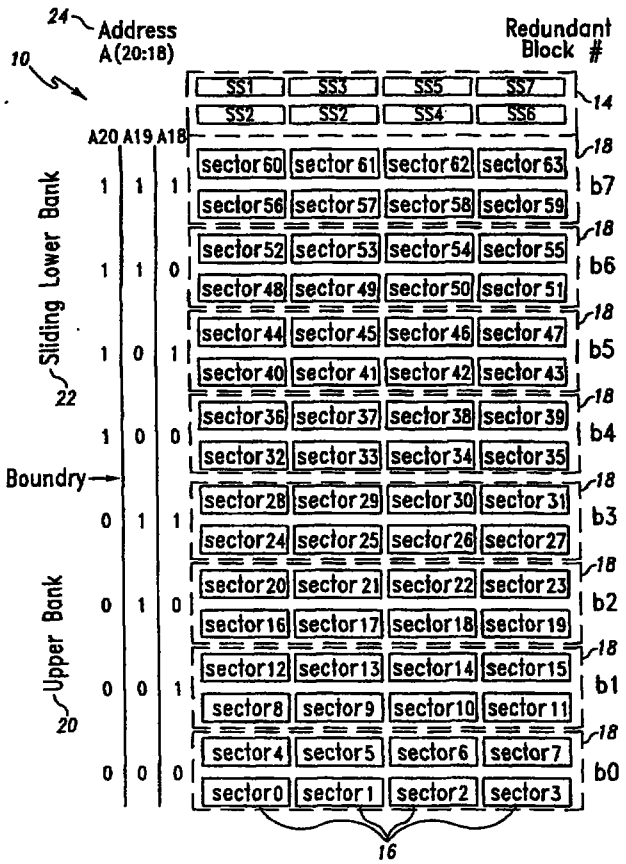
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(54) Title: REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY



(57) Abstract: The present invention discloses sector-based redundancy that is capable of making repairs using a plurality of redundant columns of memory cells in a dual bank memory device during simultaneous operation. The simultaneous operation memory device includes a plurality of redundant blocks (18) that can be configured to be located in an upper bank (20) or a sliding lower bank (22). The redundant blocks (18) are comprised of sectors (12) and each sectors (12) and each sector (12) contains columns of memory cells (26). During simultaneous operation, the memory device is capable of reading the columns of memory cells (26) in one bank and writing columns of memory cells (26) in the other bank at the same time. In addition, the simultaneous operation memory device uses sector-based redundancy to repair columns of memory cells (26) that are defective in one bank by electrically exchanging them with redundant columns of memory cells (34) and, at the same time, repair columns of memory cells (26) that are defective in the other bank. The dual bank sector-based redundancy includes a plurality of address CAM circuits (54) that are configurably associated with the redundant blocks (18) based on the blank location of the redundant blocks (18). The address CAM circuits (54) are configured by a redundancy CAM read drain decoder circuit (50).

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