CLAIMS

What is claimed is:

1. A microelectronic device comprising:

a first surface;

a second surface; and

a passageway extending from the first surface to the second surface, the passageway containing a plurality of electrically conductive channels separated from each other by an electrically insulating material.

2. The microelectronic device of claim 1 wherein:

the first surface has an electrically conductive structure attached thereto.

3. The microelectronic device of claim 1 wherein:

the second surface has an electrically conductive trace formed thereon.

4. The microelectronic device of claim 1 wherein:

the microelectronic device comprises silicon; and

the passageway is a through-silicon via.

5. The microelectronic device of claim 1 wherein:

the passageway is cylindrical; and

the electrically insulating material comprises a center portion that is centrally located within the cylindrical passageway and further comprises a plurality of arms that radiate outward from the center portion.

6. A stacked die package comprising:

a substrate;

a first microelectronic device electrically connected to the substrate and comprising:

a first surface having an electrically conductive structure attached thereto;

an opposing second surface having a metallization layer formed thereon; and

a passageway extending from the first surface to the second surface, the passageway containing a plurality of electrically conductive channels separated from each other by an electrically insulating material; and

a second microelectronic device electrically connected to the metallization layer of the first microelectronic device.

7. The stacked die package of claim 6 further comprising:

a second electrically conductive structure attached to a surface of the second microelectronic device; and

an underfill material adjacent to the second electrically conductive structure.

8. The stacked die package of claim 6 wherein:

the passageway is cylindrical; and

the electrically insulating material comprises a center portion that is centrally located within the cylindrical passageway and further comprises a plurality of arms that radiate outward from the center portion.

9. A computing system comprising:

a board;

a user interface device disposed on the board; and

a stacked die package disposed on the board, the stacked die package comprising:

a substrate;

a first microelectronic device electrically connected to the substrate and comprising:

a first surface having an electrically conductive structure attached thereto;

an opposing second surface having a metallization layer formed thereon; and

a passageway extending from the first surface to the second surface, the passageway containing a plurality of electrically conductive channels separated from each other by an electrical insulating material; and

a second microelectronic device electrically connected to the metallization layer of the first microelectronic device.

10. The computing system of claim 9 further comprising:

a second electrically conductive structure attached to a surface of the second microelectronic device; and

an underfill material adjacent to the second electrically conductive structure.

11. The computing system of claim 10 further comprising:

a third electrically conductive structure attached to the substrate, wherein the third electrically conductive structure electrically and mechanically attaches the stacked die package and the board to each other.

12. The computing system of claim 9 wherein:

the passageway is cylindrical; and

the electrically insulating material comprises a center portion that is centrally located within the cylindrical passageway and further comprises a plurality of arms that radiate outward from the center portion.

13. A method of manufacturing a multi-channel electrical communication pathway in a microelectronic device, the method comprising:

forming a passageway that extends from a first surface of the microelectronic device to a second surface of the microelectronic device;

forming a first material within the passageway;

removing portions of the first material in order to form voids within the passageway; and

forming a second material in the voids, wherein one of the first material and the second material is an electrically conductive material and the other one of the first material and the second material is an electrically insulating material, thereby isolating a plurality of electrically conductive channels within the passageway.

14. The method of claim 13 wherein:

forming the electrically conductive material comprises performing an electroless plating process in combination with an electrolytic plating process.

15. The method of claim 13 wherein:

removing portions of the first material comprises using a laser etching process.

16. The method of claim 13 wherein:

removing portions of the first material comprises forming voids that are symmetric within the passageway.

17. A method of enabling electrical communication between components of a stacked-die package, the method comprising:

providing a first microelectronic device having a first surface and a second surface;

forming a passageway that extends from the first surface to the second surface of the first microelectronic device;

forming a first material within the passageway;

removing portions of the first material in order to form voids within the passageway;

forming a second material in the voids, wherein one of the first material and the second material is an electrically conductive material and the other one of the first material and the second material is an electrically insulating material, thereby isolating a plurality of electrically conductive channels within the passageway;

forming a metallization layer on the second surface of the first microelectronic device;

attaching a second microelectronic device to the metallization layer of the first microelectronic device in order to form a stacked component made up of the first microelectronic device and the second microelectronic device; and

attaching the stacked component to a package substrate in order to form a stacked package.

18. The method of claim 17 further comprising:

attaching the stacked package to a system board.

19. The method of claim 17 wherein:

attaching the second microelectronic device to the metallization layer of the first microelectronic device comprises:

providing an electrically conductive structure at a surface of the second microelectronic device and attaching the electrically conductive structure to the metallization layer; and

providing an underfill material adjacent to the electrically conductive structure.

20. The method of claim 17 wherein:

attaching the second microelectronic device to the metallization layer of the first microelectronic device comprises using a surface activated bonding technique.

CLAIMS

1. A microelectronic device comprising:

a first surface;

a second surface; and

a passageway extending from the first surface to the second surface, the passageway containing a plurality of electrically conductive channels separated from each other by an electrically insulating material, wherein the electrically conductive channels and the electrically insulating material are in contact with the passageway.

2. The microelectronic device of claim 1 wherein:

the first surface has an electrically conductive structure attached thereto.

3. The microelectronic device of claim 1 wherein:

the second surface has an electrically conductive trace formed thereon.

4. The microelectronic device of claim 1 wherein:

the microelectronic device comprises silicon; and

the passageway is a through-silicon via.

5. The microelectronic device of claim 1 wherein:

the passageway is cylindrical; and

the electrically insulating material comprises a center portion that is centrally located within the cylindrical passageway and further comprises a plurality of arms that radiate outward from the center portion.

6. A stacked die package comprising:

a substrate;

a first microelectronic device electrically connected to the substrate and comprising:

a first surface having an electrically conductive structure attached thereto;

an opposing second surface having a metallization layer formed thereon; and

a passageway extending from the first surface to the second surface, the passageway containing a plurality of electrically conductive channels separated from each other by an electrically insulating material, wherein the electrically conductive channels and the electrically insulating material are in contact with the passageway; and

a second microelectronic device electrically connected to the metallization layer of the first microelectronic device.

7. The stacked die package of claim 6 further comprising:

a second electrically conductive structure attached to a surface of the second microelectronic device; and

an underfill material adjacent to the second electrically conductive structure.

8. The stacked die package of claim 6 wherein:

the passageway is cylindrical; and

the electrically insulating material comprises a center portion that is centrally located within the cylindrical passageway and further comprises a plurality of arms that radiate outward from the center portion.

9. A computing system comprising:

a board;

a user interface device disposed on the board; and

a stacked die package disposed on the board, the stacked die package comprising:

a substrate;

a first microelectronic device electrically connected to the substrate and comprising:

a first surface having an electrically conductive structure attached thereto;

an opposing second surface having a metallization layer formed thereon; and

a passageway extending from the first surface to the second surface, the passageway containing a plurality of electrically conductive channels separated from each other by an electrical insulating material, wherein the electrically conductive channels and the electrically insulating material are in contact with the passageway; and

a second microelectronic device electrically connected to the metallization layer of the first microelectronic device.

10. The computing system of claim 9 further comprising:

a second electrically conductive structure attached to a surface of the second microelectronic device; and

an underfill material adjacent to the second electrically conductive structure.

11. The computing system of claim 10 further comprising:

a third electrically conductive structure attached to the substrate, wherein the third electrically conductive structure electrically and mechanically attaches the stacked die package and the board to each other.

12. The computing system of claim 9 wherein:

the passageway is cylindrical; and

the electrically insulating material comprises a center portion that is centrally located within the cylindrical passageway and further comprises a plurality of arms that radiate outward from the center portion.

13. A method of manufacturing a multi-channel electrical communication pathway in a microelectronic device, the method comprising:

forming a passageway that extends from a first surface of the microelectronic device to a second surface of the microelectronic device;

forming a first material within the passageway;

removing portions of the first material in order to form voids within the passageway; and

forming a second material in the voids, wherein one of the first material and the second material is an electrically conductive material and the other one of the first material and the second material is an electrically insulating material, thereby isolating a plurality of electrically conductive channels within the passageway, wherein the electrically conductive channels and the electrically insulating material are in contact with the passageway.

14. The method of claim 13 wherein:

forming the electrically conductive material comprises performing an electroless plating process in combination with an electrolytic plating process.

15. The method of claim 13 wherein:

removing portions of the first material comprises using a laser etching process.

16. The method of claim 13 wherein:

removing portions of the first material comprises forming voids that are symmetric within the passageway.

17. A method of enabling electrical communication between components of a stacked-die package, the method comprising:

providing a first microelectronic device having a first surface and a second surface; forming a passageway that extends from the first surface to the second surface of the first microelectronic device;

forming a first material within the passageway;

removing portions of the first material in order to form voids within the passageway;

forming a second material in the voids, wherein one of the first material and the second material is an electrically conductive material and the other one of the first material and the second material is an electrically insulating material, thereby isolating a plurality of electrically conductive channels within the passageway, wherein the electrically conductive channels and the electrically insulating material are in contact with the passageway;

forming a metallization layer on the second surface of the first microelectronic device;

attaching a second microelectronic device to the metallization layer of the first microelectronic device in order to form a stacked component made up of the first microelectronic device and the second microelectronic device; and

attaching the stacked component to a package substrate in order to form a stacked package.

18. The method of claim 17 further comprising:

attaching the stacked package to a system board.

19. The method of claim 17 wherein:

attaching the second microelectronic device to the metallization layer of the first microelectronic device comprises:

providing an electrically conductive structure at a surface of the second microelectronic device and attaching the electrically conductive structure to the metallization layer; and

providing an underfill material adjacent to the electrically conductive structure.

20. The method of claim 17 wherein:

attaching the second microelectronic device to the metallization layer of the first microelectronic device comprises using a surface activated bonding technique.