

Semiconductor Device

This invention relates to a semiconductor device, and more particularly to a power transistor adapted to a high power semiconductor integrated circuit device (hereinafter referred to as a "power
5 IC").

In the power transistor in a power IC for use in an audio output circuit or the like, it is a customary practice to divide an emitter region into a plurality of regions and arrange them in one
10 base region in order to obtain a high output current. In such a power transistor, a ballast resistance is inserted between each emitter region and the single emitter input terminal so that the emitter current flows uniformly through the plurality of divided
15 emitter regions. As a method of forming this ballast resistance, it is conceivable in principle to form a resistance region with one end continuous with the emitter regions and the other end connected to the emitter input electrode, so as to reduce the
20 occupation area of the power transistor as a whole, but according to the results of experiments carried out for such a construction by the inventor of the present invention, it was found that the input electrode side of the resistance region and the resistance
25 region function as transistors. The transistor formed

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by the emitter regions of the originally intended transistor and the parasitic transistor due to the resistance region come to be co-present so that current locally concentrates in the parasitic transistor
5 due to the ballast resistance region, thus breaking down the transistor.

Accordingly, there is a need to improve the break-down strength and to increase the area of safe operation of a power transistor which uses a part
10 of its emitter regions as a ballast resistance.

According to a first aspect of the present invention, there is provided a semiconductor device including a bipolar transistor and a parasitic transistor, the semiconductor device comprising:

15 a first semiconductor region of a first conductivity type serving as a collector region of the bipolar and parasitic transistors;

a second semiconductor region of a second conductivity type serving as a base region for the
20 bipolar and parasitic transistors, the second semiconductor region being adjacent to the first semiconductor region; and

a third semiconductor region of the first conductivity type serving as an emitter region for
25 the bipolar and parasitic transistors, the third semiconductor region being adjacent to the second semiconductor region,

wherein the third semiconductor region comprises an operating portion for forming the emitter of the bipolar transistor, and a ballast resistance portion and a terminal portion which form the emitter of
5 the parasitic transistor, and further wherein the effective base width of the parasitic transistor is greater than the base width of the bipolar transistor base region in the base region portion of the parasitic transistor adjacent to the terminal portion of the
10 third semiconductor layer to reduce the current gain of the parasitic transistor, and

wherein the semiconductor device further comprises a base contact portion in the second semiconductor region extending adjacent to the operating
15 portion of the emitter region of the bipolar transistor but not extending adjacent to the ballast resistance portion and the terminal portion, an emitter electrode contacting the emitter terminal portion but not the emitter operating portion, and a base electrode
20 contacting the base contact portion so that the emitter electrode and the base electrode are spaced apart from one another.

According to a second aspect of the present invention there is provided a semiconductor device
25 including a bipolar transistor and a parasitic transistor, the semiconductor device comprising:

a first semiconductor region of a first conductivity type serving as a collector region of the bipolar and parasitic transistors;

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a second semiconductor region of a second conductivity type serving as a base region for the bipolar and parasitic transistors, said second semiconductor region being adjacent to the first semiconductor region; and

a third semiconductor region of the first conductivity type to serve as an emitter region for the bipolar and parasitic transistors, said third semiconductor region being adjacent to the second semiconductor region,

wherein the third semiconductor region comprises an operating portion for forming the emitter of the bipolar transistor and a ballast resistance portion and a terminal portion which form the emitter of the parasitic transistor, and further wherein the impurity concentration of the base region of the parasitic transistor is higher than that of the bipolar transistor base region in the base region portion of the parasitic transistor adjacent to the terminal portion of the third semiconductor layer to reduce the current gain of the parasitic transistor, and

wherein the semiconductor device further comprises a base contact portion in the second semiconductor region extending adjacent to the operating portion of the emitter region of the bipolar transistor but not extending adjacent to the ballast resistance portion and the terminal portion, an emitter electrode contacting the emitter terminal portion but not the emitter operating portion and a base electrode

contacting the base contact portion so that the emitter electrode and the base electrode are spaced apart from one another.

The accompanying drawings illustrate some
5 preferred embodiments of the present invention, wherein:-

Figure 1 is a plan view showing the power transistor portion of a power IC;

Figure 2 is a partial sectional view on the line II - II of Figure 1;

5 Figure 3 is an equivalent circuit diagram of the power transistor;

Figure 4 is a schematic sectional view useful for explaining the structure of Figure 2;

10 Figure 5 is a sectional view of the power transistor portion in another embodiment of the present invention; and

Figures 6A and 6B are sectional views showing the principal steps in fabricating the power transistor.

15 Figures 1 and 2 depict the structure of the first embodiment of power transistor. This embodiment illustrates a power transistor formed as a part of a power IC. In Figures 1 and 2, the power transistor is formed in a part of a silicon semiconductor wafer 100 consisting of a P-type substrate 1 and an N⁻-type epitaxial layer 3
20 formed on the substrate by epitaxial techniques. The portion (island region) in which the power transistor is to be formed is encompassed by an isolation region 4 and is electrically isolated from other circuit elements not shown that are to be formed on other portions of
25 the semiconductor wafer 100.

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The power transistor will be described in further detail in the following paragraphs.

5 In the epitaxial layer 3 encompassed by a P^+ isolation region 4, an annular N^+ diffusion layer 5 is formed, with a deeply extending collector electrode that reaches a buried layer 2. $\times$ P base regions 6 are formed inside the diffusion layer 5 by known diffusion techniques. As shown in the plan view of Figure 1, four base regions 6 are formed in one island region 3 and adjacent pairs of base regions 6 are encompassed by the abovementioned annular N^+ region 5. A pair of upper and lower N^+ emitter regions 7 is formed in each base region 6, as can be seen clearly from Figure 1.

15 Each emitter region 7 consists of an emitter portion 7a formed to perform the main transistor operation, a resistance portion 7b serving as the ballast resistance and an electrode extension portion 7c with which an aluminum electrode 8 serving as an emitter input terminal comes into contact. The electrode extension portion 7c contacts the electrode 8 through a contact hole 18 in a silicon oxide film 10. As schematically represented by the dot and chain line in Figure 1, this electrode 8 is connected in common with each emitter region via the contact holes 18, thereby forming the emitter input terminal.

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25 An aluminum emitter electrode 9 is in contact with the

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emitter portion 7a of the transistor operation portion via a contact hole 17. A separate emitter electrode 9 is provided for each emitter portion, independently of the others. An aluminium base electrode 14 contacts the base region 6 between a pair of emitter regions 6 via a contact hole 16. As schematically represented by the dot and chain line in Figure 1, the base electrode 14 is disposed so as to connect the base contact regions in common, thereby forming the base input terminal.

10 The collector 5 contacts on collector electrode 15.

Figure 3 is an equivalent circuit diagram of a transistor formed for one emitter region 7 of the abovementioned power transistor. Symbol Tr_1 represents a transistor formed by the emitter portion 7a and is originally intended while Tr_2 represents an undesirable parasitic transistor which is formed by the electrode extension portion 7c in contact with the emitter electrodes 8 as shown in Figure 2. Symbol R represents a ballast resistance formed by the resistance portion 7b.

20 Of specific importance here is that the region 6a of the base region 6 below the ballast resistance portion 7b and electrode extension portion 7c is formed so as to protrude downwardly, and the effective base width of the parasitic transistor Tr_2 is increased in comparison with the width of the other portions.

25 Referring to Fig. 4, if the original base width d_1 is about $1\mu m$, for instance the width d_2 by which

the base portion 6a protrudes downwardly may be about 1 μ m and this depth of protrusion may be such as to provide a withstand voltage.

As described above, the current gain h_{FE} of the parasitic transistor Tr_2 can be reduced by increasing its base width. Accordingly, current concentration on that portion during the transistor operation can effectively be prevented and it becomes possible to flow current through the original transistor Tr_1 . Moreover, since the original transistor Tr_1 has an ordinary base width, its characteristics are not deteriorated. The emitter ballast resistance prevents current concentration in the specific emitter region or regions 7a and the current is uniformly distributed to the emitters of the divided emitter regions. Accordingly, the break-down strength of the transistor as a whole or as a power transistor can be markedly improved and the characteristics of the original transistor can be maintained satisfactorily due to the existence of the expanded base width portion 6a.

This expanded base width portion 6a may be formed longitudinally as a whole with respect to one base region 6 in Figure 1. Alternatively, separate expanded base width portions may be disposed so as to correspond to each emitter region of a pair of transistors formed inside one base region 6. The expanded base width portion 6a may be formed by forming a p^+ region

in advance at a position corresponding to the expanded base width portion 6a by a diffusion technique or an ion-implantation technique and then performing the base diffusion. This p^+ region can be formed simultaneously with the formation of a p^+ region in a lateral PNP transistor or a zener diode elsewhere in the I.C.

Figures 5, 6A and 6B illustrate another embodiment in accordance with the present invention, in which the same reference numerals are used to identify the same constituents as in the above embodiment and explanation of such constituents will not be repeated.

In this embodiment, the base width is uniform for both transistors Tr_1 and Tr_2 , as shown in Figure 5. However, a p^+ region 6b of a relatively higher concentration than the other base regions is formed in a part of the base region 6 associated with the parasitic transistor Tr_2 . To improve the collector-to-base withstand voltage, it is preferred that this p^+ region 6b be disposed to an intermediate depth in the base region 6 so that it does not come into contact with the collector region 3, though it does contact the emitter region 7.

The p^+ region 6b can be formed in the following manner. First, as shown in Figure 6A, the base region 6 is formed by the diffusion technique and a part of the SiO_2 film 10 is removed by etching. A P type impurity such as boron ion

12 is then implanted into a region corresponding to the parasitic transistor through the aperture 11 thus defined, in a dose of about $5 \times 10^{13 \sim 14} \text{ cm}^{-2}$, for example. Next, after forming a window for impurity introduction in the SiO_2 film 10, an impurity diffusion is effected in order to form the ordinary emitter region 7, as shown in Figure 6B. Simultaneously with the diffusion of this emitter region, the P type impurity in the ion implantation region 13 is pushed below the emitter region 7. Thus, the P^+ type region 6b which is expanded locally within the base region 6 is formed immediately below the resistance portion 7b and contact portion 7c of the emitter region and around their periphery. This P^+ type region 6b has a higher concentration than that of the original base region 6 and has a sheet resistance of up to $200 \Omega/\square$, for instance, but the resistance is smaller than that of the other base regions.

In the abovementioned manner, if the high concentration region 6b is disposed inside the base region of the parasitic transistor, h_{FE} of the parasitic transistor can be reduced so that the current concentration can be prevented and the breakdown strength can be improved. Since the P^+ type region 6b does not affect the other base regions, the characteristics of the original transistor are not deteriorated. Further, since this P^+ type region 6b is formed after passing through the abovementioned ion implantation process, its impurity concentration has a higher concentration peak on the side

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closer to the emitter side than the other base regions. As the result of this, the region 6b contributes to reduce h_{FE} of the parasitic transistor.

Though the present invention has thus been
5 described with reference to the preferred embodiments thereof, the embodiments can be further modified on the basis of the technical concept of the present invention. For example, the position, shape and size of each of the expanded base width portion 6a
10 or the high concentration region may be changed in various manners, as may the methods of forming them. The current gain can also be controlled by increasing the impurity concentration of the expanded portion 6a. Furthermore, another region or regions or means
15 for reducing the current gain may be formed on the base of the parasitic transistor. Additionally, the present invention can be applied to form a PNP transistor by changing the semiconductor type of each of the abovementioned semiconductor regions.

20 As described in the foregoing, since current gain is reduced by greater base width or higher impurity concentration of the base region, of the parasitic transistor it becomes possible to prevent current concentration in the parasitic transistor
25 and to improve the breakdown strength of the transistor as a whole so the transistor can operate in a satisfactory

manner without deteriorating the characteristics of the originally intended transistor. Thus, it is possible to provide a semiconductor device which is extremely useful especially as a power transistor.

5 U.K. Patent Application No. 84.28941 has been divided out of the present application and describes matter also disclosed in the present application. Attention is drawn to that application.

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CLAIMS:

1. A semiconductor device including a bipolar transistor and a parasitic transistor, the semiconductor device comprising:

5 a first semiconductor region of a first conductivity type serving as a collector region of the bipolar and parasitic transistors;

a second semiconductor region of a second conductivity type serving as a base region for the bipolar and parasitic transistors, the second semiconductor
10 region being adjacent to the first semiconductor region; and

a third semiconductor region of the first conductivity type serving as an emitter region for the bipolar and parasitic transistors, the third
15 semiconductor region being adjacent to the second semiconductor region,

wherein the third semiconductor region comprises an operating portion for forming the emitter of the bipolar transistor, and a ballast resistance portion
20 and a terminal portion which form the emitter of the parasitic transistor, and further wherein the effective base width of the parasitic transistor is greater than the base width of the bipolar transistor base region in the base region portion of the parasitic
25 transistor adjacent to the terminal portion of the third semiconductor layer to reduce the current gain of the parasitic transistor, and



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wherein the semiconductor device further comprises a base contact portion in the second semiconductor region extending adjacent to the operating portion of the emitter region of the bipolar transistor but not extending adjacent to the ballast resistance portion and the terminal portion, an emitter electrode contacting the emitter terminal portion but not the emitter operating portion, and a base electrode contacting the base contact portion so that the emitter electrode and the base electrode are spaced apart from one another.

2. A semiconductor device according to claim 1 wherein the effective base width of the parasitic transistor is approximately twice the base width of the bipolar transistor base region.

3. A semiconductor device according to claim 1 wherein the said bipolar transistor is a first bipolar transistor, the said parasitic transistor is a first parasitic transistor, the device also having a second bipolar transistor and a second parasitic transistor,

wherein the first semiconductor region serves as a common collector region of the first and second bipolar and the first and second parasitic transistors, the second semiconductor region serves as a common base region for the first and second bipolar and the first and second parasitic transistors,



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a fourth semiconductor region of the first conductivity type serves as an emitter region for the second bipolar and the second parasitic transistors the fourth semiconductor region being adjacent to the second semiconductor region;

wherein the fourth semiconductor region comprises an operating portion for forming the emitter of the second bipolar transistor, and a ballast resistance portion and a terminal portion which form the emitter of the second parasitic transistor, and further wherein the effective base width of the second parasitic transistor is greater than the base width of the second bipolar transistor base region in the base region portion of the second parasitic transistor adjacent to the terminal portion of the fourth semiconductor layer to reduce the current gain of the second parasitic transistor; and

wherein the base contact portion is between the third and fourth semiconductor regions and extends adjacent to said operating portions of said emitters of the first and second bipolar transistors but not adjacent to the ballast resistance portions and the terminal portions of the third and fourth regions, the emitter electrode contacts the emitter terminal portions of both the third and fourth regions but not the emitter operating portions of the third and fourth regions, and the base electrode contacts the base contact regions.



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4. A semiconductor device according to claim 1 or claim 2, wherein the said bipolar transistor is a first bipolar transistor, the said parasitic transistor is a first parasitic transistor, the device
5 also having a second bipolar transistor and a second parasitic transistor;

wherein the first semiconductor region serves as a common collector region of the first and second bipolar and the first and second parasitic transistors;

10 a fourth semiconductor region of the first conductivity type serves as an emitter region for the second bipolar and the second parasitic transistors, .

and a fifth semiconductor region of the second conductivity type serves as a base region for the
15 second bipolar and second parasitic transistors, said fifth semiconductor region being adjacent to the first semiconductor region; and

wherein the fourth semiconductor region comprises an operating portion for forming the emitter of the
20 second bipolar transistor, and a ballast resistance portion and a terminal portion which form the emitter of the second parasitic transistor, and further wherein the effective base width of the second parasitic transistor is greater than the base width of the
25 second bipolar transistor base region in the base



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region portion of the second parasitic transistor adjacent to the terminal portion of the fourth semiconductor region to reduce the current gain of the second parasitic transistor; and

5 wherein the said base contact portion is a first base contact portion, and there is a second base contact in the fifth semiconductor region extending adjacent to the operating portion of the emitter of the second bipolar transistor but not extending
10 adjacent to the ballast resistance portion and the terminal portion of the fourth semiconductor region, the emitter electrode contacts the emitter terminal portions of both the third and fourth semiconductor regions but not the emitter operating portions of
15 the third and fourth semiconductor regions, and the base electrode contacts the first and second base contact portions.

5. A semiconductor device including a bipolar transistor and a parasitic transistor, the semiconductor
20 device comprising;

 a first semiconductor region of a first conductivity type serving as a collector region of the bipolar and parasitic transistors;

 a second semiconductor region of a second
25 conductivity type serving as a base region for the bipolar and parasitic transistors, said second semiconductor region being adjacent to the first semiconductor region; and



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a third semiconductor region of the first conductivity type to serve as an emitter region for the bipolar and parasitic transistors, said third semiconductor region being adjacent to the second semiconductor
5 region,

wherein the third semiconductor region comprises an operating portion for forming the emitter of the bipolar transistor and a ballast resistance portion and a terminal portion which form the emitter of
10 the parasitic transistor, and further wherein the impurity concentration of the base region of the parasitic transistor is higher than that of the bipolar transistor base region in the base region portion of the parasitic transistor adjacent to the terminal
15 portion of the third semiconductor layer to reduce the current gain of the parasitic transistor, and

wherein the semiconductor device further comprises a base contact portion in the second semiconductor region extending adjacent to the operating portion
20 of the emitter region of the bipolar transistor but not extending adjacent to the ballast resistance portion and the terminal portion, an emitter electrode contacting the emitter terminal portion but not the emitter operating portion and a base electrode
25 contacting the base contact portion so that the emitter electrode and the base electrode are spaced apart from one another.

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6. A semiconductor device according to claim 5 wherein said higher impurity concentration base region of the parasitic transistor is in the second semiconductor region, and underlies said terminal portion of the emitter but does not underlie the operating portion of the emitter, and wherein the higher impurity concentration base region of the parasitic transistor does not directly contact the first semiconductor region.
- 10 7. A semiconductor device according to claim 5 or claim 6, wherein the said bipolar transistor is a first bipolar transistor, the said parasitic transistor being a first parasitic transistor, the device also having a second bipolar transistor and a second
- 15 parasitic transistor,
- wherein the first semiconductor region serves as a common collector region of the first and second bipolar and the first and second parasitic transistors the second semiconductor region serves as a common
- 20 base region for the first and second bipolar and the first and second parasitic transistors, a fourth semiconductor region of the first conductivity type serves as an emitter region for the second bipolar and the second parasitic transistors, the fourth
- 25 semiconductor region being adjacent to the second semiconductor region;



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wherein the fourth semiconductor region comprises an operating portion for forming the emitter of the second bipolar transistor, and a ballast resistance portion and a terminal portion which form the emitter
5 of the second parasitic transistor, and further wherein the impurity concentration of the base region of the second parasitic transistor is greater than that of the second bipolar transistor base region in the base region portion of the second parasitic transistor
10 adjacent to the terminal portion of the fourth semiconductor layer to reduce the current gain of the second parasitic transistor; and

wherein the base contact portion is between the third and fourth semiconductor regions and extends
15 adjacent to the operating portions of the emitters of the first and second bipolar transistors but not extending adjacent to the ballast resistance portions and the terminal portions of the third and fourth regions, the emitter electrode contacts the emitter
20 terminal portions of both the third and fourth regions but not the emitter operating portions of the third and fourth regions, and the base electrode contacts the base contact regions.

8. A semiconductor device according to claim
25 5 or claim 6, wherein the said bipolar transistor is a first bipolar transistor, the said parasitic transistor is a first parasitic transistor, the device also having a second bipolar transistor and a second parasitic transistor;

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wherein the first semiconductor region serves as a common collector region of the first and second bipolar and the first and second parasitic transistors,

a fourth semiconductor region of the first conductivity type serves as an emitter region for the second bipolar and the second parasitic transistors, and a fifth semiconductor region of the second conductivity type serves as a base region for the second bipolar and second parasitic transistors, the fifth semiconductor region being adjacent to the first semiconductor region;

wherein the fourth semiconductor region comprises an operating portion for forming the emitter of the second bipolar transistor, and a ballast resistance portion and a terminal portion which form the emitter of the second parasitic transistor, and further wherein the impurity concentration of the base region of the second parasitic transistor is higher than that of the second bipolar transistor base region in the base region portion of the second parasitic transistor adjacent to the terminal portion of the fourth semiconductor region to reduce a current gain of the second parasitic transistor; and

wherein the base contact portion is a first base contact portion, and there is a second base contact portion in the fifth semiconductor region



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extending adjacent to the operating portion of the emitter of the second bipolar transistor but not extending adjacent to the ballast resistance portion and the terminal portion of the fourth semiconductor region, the emitter electrode contacting the emitter terminal portions of both the third and fourth semiconductor regions but not the emitter operating portions of the third and fourth semiconductor regions, and the base electrode contacting the first and second base contact portions.

9. A semiconductor device according to claim 4 or claim 8, wherein the fourth semiconductor region is within the fifth semiconductor region.

10. A semiconductor device according to claim 3 or claim 7, wherein the fourth semiconductor region is within the second semiconductor region.

11. A semiconductor device according to any one of the preceding claims, wherein the third semiconductor region is within the second semiconductor region, and the second semiconductor region is within the first semiconductor region.

12. A semiconductor device substantially as herein described with reference to and as illustrated in Figs. 1 to 4 or Fig. 5 or Figs. 6A and 6B of the accompanying drawings.
