CLAIMS

1. An apparatus comprising: at least two sources; at least two memory arrays respectively formed over and coupled to the at least two sources, wherein each of the at least two memory arrays includes vertical strings of memory cells, control gates, and data lines; and a source conductor coupled to the at least two sources respectively using source contacts adjacent source edges, wherein there is no data line between a source edge of the source edges and a source contact of the source contacts for each of the at least two sources, wherein each of the source contacts includes a first contact electrically coupled to the source conductor, a second contact electrically coupled to a source of the at least two sources, and a conductive connector connecting the first and second contacts.

2. The apparatus of claim 1, wherein each of the at least two sources comprises metal material.

3. The apparatus of claim 1, wherein each of the at least two sources comprises WSi.

4. The apparatus of claim 1, wherein each of the at least two sources comprises a stack of metal material and polysilicon.

5. The apparatus of claim 1, wherein each of the at least two sources comprises a stack of polysilicon and WSi.

6. An apparatus comprising: a source; a memory array formed over and coupled to the source, the memory array including vertical strings of memory cells, control gates, and data lines; and a source conductor coupled to the source through a source contact adjacent an edge of the source, wherein there is no data line between the edge of the source and the source contact, wherein the source conductor extends over the memory array, and further comprising an interconnection component extending perpendicular to the source conductor and coupled to the source conductor using an interconnection contact.

7. The apparatus of claim 6, wherein the source contact comprises a plurality of source contacts, and further wherein there is no source routing inside the memory array.

8. The apparatus of claim 6, wherein the source contact is adjacent the edge of the source in a control gate direction.

9. The apparatus of claim 6, wherein the source contact is adjacent the edge of the source on a side of and between groups of control gate contacts.

10. The apparatus of claim 6, wherein the source contact is adjacent the edge of the source on a side opposite to groups of control gate contacts.

11. The apparatus of claim 6, wherein the source contact comprises a first source contact, and wherein a second source contact is adjacent another edge of the source.

12. The apparatus of claim 6, wherein the interconnection component extends below the source.

13. The apparatus of claim 6, wherein the source extends between the source conductor and the interconnection component.

14. The apparatus of claim 6, wherein the interconnection contact includes a first contact electrically coupled to the source conductor, a second contact electrically coupled to the interconnection component, and a third contact connecting the first contact and the second contact.

15. The apparatus of claim 6, wherein the interconnection component extends over the source conductor.

16. The apparatus of claim 6, wherein the source conductor extends between the interconnection component and the source.

17. The apparatus of claim 6, wherein the interconnection contact comprises a single conductive plug.

18. The apparatus of claim 6, wherein the control gates comprise a plurality of tiers of a first semiconductor material.

19. The apparatus of claim 18, wherein the first semiconductor material comprises polysilicon.

20. The apparatus of claim 19, wherein the memory array comprises a plurality of vertical pillars of a second semiconductor material.

21. The apparatus of claim 20, wherein the second semiconductor material comprises polysilicon.

22. An apparatus comprising: at least two sources; at least two memory arrays respectively coupled to the at least two sources, each of the at least two memory arrays including memory cells, control gates, and data lines; a source conductor over the at least two memory arrays, and coupled to the at least two sources through source contacts adjacent edges of the at least two sources; and a signal conductor

parallel with the source conductor, and coupled to gates of transistors to provide control signals to the at least two memory arrays.

23. The apparatus of claim 22, wherein the transistors are formed on a same semiconductor substrate.

24. The apparatus of claim 23, wherein the semiconductor substrate comprises silicon.

25. The apparatus of claim 1, wherein the at least two memory arrays and the source conductor are included in a memory device, and wherein the memory device is coupled to a memory controller and/or a processor to send a control signal to the at least two memory arrays.

26. The apparatus of claim 1, wherein there is no source routing inside any of the at least two arrays.