Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a photoelectric conversion device having photoelectric conversion cells wherein potential at the control electrode region of the transistor is controlled through a capacitor, carriers generated upon light excitation at the control electrode are stored to control the output of the transistor by the potential generated by the stored carriers.

Related Background Art

Fig. 1A is a diagrammatical cross section of a photoelectric conversion device disclosed in EP Laid-open Publication No. 132076, and Fig. 1B is a equivalent circuit of a photoelectric conversion cell of the device.

In the figures, photoelectric conversion cells are disposed on an n^+ silicon substrate 1, each photoelectric conversion cell being electrically isolated from adjacent cells by an element isolation region 2 made of materials such as SiO_2, Si_3N_4 or polysilicon.

Each photoelectric conversion cell is constructed as in the following.

On an n^- region 3 having a low concentration of the impurity and formed using the epitaxial technology or the like, a p region 4 is formed by doping p-type impurities into the n^- region 3. An $^+$ region 5 is formed with the p region 4 using the impurity diffusion technology, or ion implanting technology. The p region 4 and N^+ region 5 respectively correspond to the base and emitter of the bipolar transistor.

Formed on the n^- region 3 is an oxidation layer 6 on which a capacitor electrode 7 having a predetermined area is formed. The capacitor electrode 7 confronts the p region 4, the oxidation layer 6 being interposed therebetween, and controls potential of the floating p region 4 by applying a pulse voltage thereto.

Also formed on the photoelectric conversion device are an emitter electrode 8 connected to the n^+ region 5, an n^+ region 11 having a high concentration of the impurity and formed on the back of the substrate 1, and a collector electrode 12 for supplying a collector potential to the bipolar transistor.

Next, the fundamental operation of the photoelectric conversion device will be described. It is assumed that the p region 4 serving as the base of the bipolar transistor has a negative potential at its initial condition. Light 13 is applied to the p region 4 to generate pairs of electrons and holes. Holes are stored in the p region 4 so that the potential of the p region 4 changes positive (store operation).

In this condition, a positive pulse voltage is applied to the capacitor electrode 7 for reading light information. That is, a signal or light information corresponding to the base potential change during the store operation is outputted from the electrode 8 of the floating emitter (read operation). In this case, a non-destructive read is possible since the stored charge in the base or p region 4 scarcely reduces.

To remove holes stored in the p region 4, the emitter electrode is grounded and the capacitor electrode 7 is applied with a positive refresh pulse voltage. Upon application of this pulse the p region 4 is forward biased relative to the n^+ region 5 to accordingly remove stored holes. After the refresh pulse falls, the p region 4 resumes the initial condition of negative potential (refresh operation). Thereafter, similar store, read and refresh operations are repeated.

In summary, according to the above method, carriers generated by incident light are stored in the base or p region 4, and current passing between the emitter electrode 8 and the collector electrode 12 is controlled by the quantity of stored charges. Since stored carriers are amplified by amplification function of the cell itself, a large output, high sensitivity and low noise can be realized.

Base potential Vp generated by light-excited carriers of the base is given by Q/C, where Q is the charge quantity of carriers stored in the base, and C is the capacitance of the base. As the cell size becomes small due to high integration density, the values of Q and C becomes small. Thus, as apparent from the formula, the potential Vp generated by light excitation remains substantially constant. Therefore, it can be said that the above-proposed method is advantageous for obtaining a high resolution of the device.

With such a photoelectric conversion device, only light information stored in a photoelectric conversion cell is read from the emitter electrode. Therefore, it is necessary to measure the quantity of light or detect a peak value prior to a read operation, resulting in an obstacle to high speed operation. Further, there arises a problem that the circuit for regulating exposure time and gain based on the detected value becomes complicated in its construction and operation.

DE-A-3345190 discloses a photosensitive static induction transistor (SIT), having high impurity concentration source and drain regions and a low impurity concentration channel region, all of the same conductivity type. A signal control gate region, of the other impurity type, is in contact with the channel region but not with the source or drain

regions. The signal control gate region is capacitively coupled to an electrode. Photo-induced carriers are stored in the signal control gate. A further region, of the same conductivity type as the drain, source and channel regions, is formed within the signal control gate region, and is directly connected to a further electrode. In another embodiment, the further region is not provided in the signal control gate region, but is instead provided in an isolation gate region of the same conductivity type as the signal control gate region, the isolation gate region being directly connected to an electrode.

US-A-3660667 discloses an image sensor array in which each cell comprises a double emitter bipolar transistor. The pn junction capacitances of the emitters with the base region are very different. Charge is stored on the pn junction capacitances between the emitters and the base, and is discharged by received light. The emitter having the larger junction capacitance is never forward biased. The light signal is read by forward biasing the other emitter, so that a re-charging current flows to the junction capacitances, the magnitude of the recharging current being related to the quantity of received light. Row select signals are applied to the emitter having the larger capacitance.

US-A-4471228 discloses an image sensor in which selected cells of an array are read non-destructively to an exposure detector, in addition to the cells being read by a scanner. Each cell can only be read out through a single semiconductor region and output electrode.

Attention is directed to our co-pending application EP-A-0222624, which discloses a structure having some similarities to the structure disclosed herein.

SUMMARY OF THE INVENTION

According to the present invention there is provided a photoelectric conversion cell as set out in claim 1, and a photoelectric conversion device comprising such cells as set out in claim 2. The remaining claims set out optional features.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a diagrammatical cross section of a photoelectric conversion device disclosed in EP Laid-open Publication no. 132076;

Fig. 1B is an equivalent circuit of a photoelectric conversion cell of the device shown in Fig. 1A;

Fig. 2A is a diagrammatical plan view of an embodiment of the photoelectric conversion device according to the present invention;

Fig. 2B is a cross section along line A-A of Fig. 2A;

Fig. 2C is an equivalent circuit of a photoelectric conversion element of the device shown in Figs. 2A and 2B;

Fig. 3A is a circuit diagram showing an example of an image pickup device using the embodiment of the present invention;

Fig. 3B is a timing chart illustrating the operation of the image pickup device;

Fig. 4A is a circuit diagram showing another example of an image pickup device using the embodiment of the present invention; and

Fig. 4B is a timing chart illustrating the operation of the image pickup device shown in Fig. 4A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention will now be described with reference to the accompanying drawings.

Fig. 2A is a diagrammatical plan view of an embodiment of the photelectric conversion device according to the present invention, Fig. 2B is a cross section along line A-A of Fig. 2A, and Fig. 2C is an equivalent circuit of a photoelectric conversion element of the device shown in Figs. 2A and 2B. Like regions and elements having the same function as of the example of Fig. 1 have been designated using identical numerals, and the description therefore is omitted.

In the figures, a p base region 4 is formed in an n^- epitaxial layer 3, and n^+ emitter regions 5 and 5' are formed in the p base region 4. Emitter electrodes 8 and 8' are connected to the n^+ regions 5 and 5', respectively.

In this embodiment, an element isolation region 2 is constructed of an insulation region 14 and an n^+ region 15 formed just under the insulation region 14, and electrically isolates adjacent photoelectric conversion cells.

A capacitor electrode 7 is formed on the p base region 4 an oxidation layer 6 being interposed therebetween. The areas where the capacitor electrode and emitter electrodes are formed, and shielded from light by a light shielding layer 17 so that a light receiving surface is formed on the main area of the p base region 4. A passivation layer 18 is formed on the light shielding layer 17 and the insulation layer 16 which serves as the light receiving surface.

In this embodiment, two emitter regions have been formed. The present invention, however, is not limited threreto but a plurality of emitter regions may be formed for specific purposes.

The fundamental operation of this embodiment, including store, read and refresh operations, is similar to that disclosed in the above EP Laid-open Publication. However, with this embodiment, light

information can be separately read because two emitter regions are formed, and this enables application to the following image pickup device.

Fig. 3A is a circuit diagram showing an example of an image pickup device using the embodiment of the present invention, and Fig. 3B is a timing chart illustrating the operation of the image pickup device.

In the figures, n photoelectric conversion cells 20-1 to 20-n are disposed in one-dimensionally, the collector electrodes 12 of the cells being connected in common to which a positive voltage or a ground potential is applied. Capacitor electrodes 7 are connected in common via a line 23 to a terminal 24 to which a signal ϕ_r for read or refresh operation is applied. Ones of the emitters 8 are respectively connected to vertical lines 21-1 to 21-n, while the others of the emitters 8' are connected to a common line 22.

The vertical lines 21-1 to 21-n are grounded via respective transistors 25-1 to 25-n. The gate electrodes of the transistors 25-1 to 25-n are connected in common via line 26 to a terminal 27 to which a signal ϕ_{vs} is applied.

The vertical lines 21-1 to 21-n are also respectively connected to one main electrodes of transistors 28-1 to 28-n, which are connected in common via line 29 to a terminal 30 to which a signal ϕ_t is applied. The other main electrodes of the transistors 28-1 to 28-n are respectively grounded via charge store capacitors 31-1 to 31-n, and are respectively connected to an output line 35 via transistors 34-1 to 34-n.

The gate electrodes of the transistors 34-1 to 34-n are respectively connected to parallel output terminals 33-1 to 33-n of a shift register 32, signals ϕ_1 to ϕ_n being outputted from the parallel output terminals.

The output line 35 is grounded via a transistor 36 which resets the output line 35, and connected to the gate electrode of a transistor 39 serving as an output amplifier. The gate electrode of the reset transistor 36 is connected via a line 37 to a terminal 38 to which a signal ϕ_{hs} is applied. One main electrodes of the transistor 39 are connected to a positive voltage terminal 41, while the other main electrodes are connected via a resistor 40 to a negative voltage terminal 42. The other main electrodes are also connected to the input terminal of an amplifier 43 which outputs read light information from its output terminal 44. A capacitor coupling the amplifier 43 may be omitted depending on the potential of an operating point.

The common line 22 is grounded via transistor 46, and connected to the input terminal of an amplification regulating circuit 45. The gate electrode of the transistor 46 is connected via the line 37 to a terminal 38 to which the same signal ϕ_{hs} applied to the transistor 36 is applied. The output terminal of the amplification regulating circuit 45 is connected to an amplification select terminal of the amplifier 43 which regulates the amplification factor of the amplifier based on an input signal from the common line 22.

The operation of the embodiment thus constructed will be described with reference to Fig. 3B.

(Refresh Operation)

First, the transistors 25-1 and 25-n and reset transistors 36 and 46 are rendered ON by applying high level signals of ϕ_{vs} and ϕ_{hs}. Then, the emitter electrodes 8 and 8' of the photoelectric conversion cells 20-1 and 20-n become grounded. Succeedingly, at time t_1, the signal ϕ_t becomes high level to make the transistors 28-1 to 28-n turn ON so that the charge store capacitors 31-1 to 31-n become grounded to thereby remove residual charges. Thereafter, at time t_2, the pulse signal ϕ_t falls and the signal ϕ_r becomes high level so that a positive refresh voltage is applied to the capacitor electrodes of the photoelectric conversion cells 20-1 to 20-n. Since the emitter electrodes 8 and 8' are being grounded, a refresh operation is achieved as previously described. When the signal ϕ_r falls at time t_3, the base region 4 of each photoelectric conversion cell resumes its initial condition. After a refresh operation, the signals ϕ_{vs} and ϕ_{hs} fall, and the transistors 25-1 and 25-n and 28-1 and 28-n become turned OFF.

(Store Operation)

With the above condition, holes among pairs of electron and holes generated by incident light are stored in the base region 4 of each photoelectric conversion cell 20-1 to 20-n, so that the base potential of each cell rises from its initial negative potential, by the amount of the stored voltage corresponding to the incident light quantity.

(Read Operation)

After performing a store operation for a desired time, first the signal ϕ_t is rendered high level to make the transistors 28-1 to 28-n turn ON. Thus, the vertical lines 21-1 to 21-n are respectively made connected to charge store capacitors 31-1 to 31-n.

Succeedingly, at time t_4, the signal ϕ_r rises to apply a read positive voltage to the capacitor electrode 7 of each photoelectric conversion cell. Thus, a read operation as described previously is performed where light information of the photoelectric conversion cells 20-1 to 20-n is read and stored in the charge store capacitors 31-1 to 31-n and deliv-

ered onto the common line 22.

In this case, light information of the photoelectric conversion cells 20-1 to 20-n is read and stored in the respective charge store capacitors 31-1 to 31-n, whereas on the common line 22, the light information of the photoelectric conversion cells to which the largest quantity of incident light has been applied, appears as a peak voltage. Based on this peak voltage, the amplification regulating circuit 45 regulates the amplification factor of the amplifier 43 to suppress a signal quantity difference between high and low level light signals and realize an automatic stop.

After completion of regulating the amplification factor of the amplifier 43, the signals ϕ_r and ϕ_t fall, and the pulse signal ϕ_{hs} is applied to the terminal 38. Then, the transistors 28-1 to 28-n are rendered OFF, and the common line 22 and the output line 35 are reset.

Thereafter, from time t_5, the shift register 32 is activated to sequentially read stored light information from the charge store capacitors 31-1 to 31-n. First, when the signal ϕ_1 outputted from the output terminal 33-1 of the shift register 32 becomes high level, the transistor 34-1 is rendered ON so that the light information stored in the charge store capacitor 31-1 is read onto the output line 35. The readout light information is inputted via the transistor 39 to the amplifier 43, whose amplification factor has already been regulated, and outputted from the terminal 44. Succeedingly, when the signal ϕ_1 falls, the signal ϕ_{hs} becomes high level so that the output line 35 is made grounded via the transistor 36 to thereby remove residual charges.

Similarly, the signals ϕ_2 to ϕ_n outputted from the shift register 32 sequentially become high level, light information stored in the charge store capacitors 31-2 to 31-n are sequentially read and the output line 35 is reset every time light information is read and the signal ϕ_{hs} becomes high level. In such a manner, light information of all the photoelectric conversion cells 20-1 to 20-n is serially outputted from the amplifier 43 with a regulated amplification factor. The refresh, store and read operations are repeated in the similar manner as above, during which a peak value is detected every time a read operation is to be performed, to regulate the amplification factor of the amplifier 43.

As appreciated, since a read operation for light information and a peak value detecting operation are carried out in parallel, it is possible to achieve a high speed operation as a whole.

Fig. 4A is a circuit diagram showing another example of an image pickup device using the embodiment of the present invetion, and Fig. 4B is a timing chart illustrating the operation of the image pickup device shown in Fig. 4A. Like elements to those in the circuit of Fig. 3A have been designated using identical symbols or numerals, and the description therefor is omitted.

Referring to Fig. 4A, bipolar transistors of photoelectric conversion cells 20-1 to 20-n have a current amplification factor sufficiently large enough for reducing carrier decay in a base region 4, as described later. Emitter electrodes 8' of the photoelectric conversion cells 20-1 to 20-n are connected in common to a common line 22, grounded via reset transistor 46, and connected to a control circuit 48. The gate electrode of the transistor 46 is connected to a terminal 27 to which a signal ϕ_{vs} is applied.

The control circuit 48 outputs signals ϕ_t and ϕ_r to lines 29 and 23, respectively. As described later, the signal ϕ_t during a read operation is outputted when a volgage Vpk at the common line 22 reaches a set voltage v_0. The control circuit 48 also outputs a control signal to a shift register 32.

The remaining circuit arrangement is the same as that of the circuit shown in Fig. 3A except the amplifier 43 and the amplification regulating circuit 45.

Next, the operation of the image pickup device constructed as above will be described with reference to Fig. 4B.

First, the transistors 25-1 and 25-n and reset transistors 36 and 46 are rendered ON by applying high level signals of ϕ_{vs} and ϕ_{hs}. Then, the emitter electrodes 8 and 8' of the photoelectric conversion cells 20-1 and 20-n are grounded so that the potential Vpk of the common line 22 takes a ground potential.

Succeedingly, at time t_1, the signal ϕ_t becomes high level to make the transistors 28-1 to 28-n turn ON so that the charge store capacitors 31-1 to 31-n are made grounded to remove residual charges. Thereafter, after the pulse signal ϕ_t falls, the signal ϕ_r becomes high level at time t_2 so that a positive refresh voltage is applied to the capacitor electrodes of the photoelectric conversion cells 20-1 to 20-n. Since the emitter electrodes 8 and 8' are being grounded, a refresh operation is achieved as previously described.

The refresh operation terminates at time t_3, with the signals ϕ_{vs} and ϕ_{hs} fall and the transistors 25-1 to 25-n and 28-1 to 28-n being rendered OFF. However, the signal ϕ_r remains high level so that the capacitor electrode 7 of each photoelectric conversion cell continues to be applied with a positive voltage. When a store operation starts in this condition, a read operation is also carried out in parallel so that light information voltages corresponding to the incident light quantities appear at the emitter electrodes 8 and 8'. In this case, although the holes stored in the base region 4 of each photoelectric conversion cell decays due to recombination of $1/h_{fe}$, the decay of holes by recom-

bination can be neglected because of a sufficiently large current amplification factor h_{fe}.

Each emitter electrode 8 takes a voltage of each light information of the photoelectric conversion cells 20-1 to 20-n because the transistors 28-1 to 28-n and 25-1 to 25-n are being OFF. Contrary to this, each emitter electrode 8' takes a peak voltage Vpk among those light information because the emitter electrode 8' is connected to the common line 22.

A change in the peak voltage Vpk is detected by the control circuit 48. When the peak voltage Vpk reaches a preset voltage V_0 (time t_4), the control circiut 48 makes the signal ϕ_t high level and makes the transistors 28-1 to 28-n turn ON. Then, the store operation terminates where light information appearing at the vertical lines 21-1 to 21-n is stored in the charge store capacitors 31-1 to 31-n. The following operation (after time t_5) for sequentially outputting light information stored in the charge store capacitors 31-1 to 31-n, is similar to that of the first example shown in Fig. 3B.

In the second example of the image pickup device, a peak voltage Vpk is detected from the emitter electrode 8', and the period of a store operation is controlled based on the peak voltage Vpk. Therefore, similar to the first example, it is possible to suppress the signal quantity difference between high and low level light signals and realize an automatic stop function. It is obvious that the second example can be applied to the first example to regulate the amplification factor of the amplifier 43 based on the peak voltage Vpk.

In the above embodiment, although the photoelectric conversion cells have been disposed one-dimensionally as a line sensor, obviously the present invention is also applicable to an area sensor having cells disposed two-dimensionally.

As seen from the foregoing description, the photoelectric conversion device according to the present invention can read light information from a semiconductor region provided separately from the electrode region. Therefore, light information can be read from the main electrode region and also from the semiconductor region. Thus, semiconductor region can be used, for example, in measuring the incident light quantity or detecting a peak value. Consequently, the measuring the incident light quantity or detecting a peak value can be carried out in parallel with such as a store operation or a read operation, resulting in a high speed operation of the device. Further, use of a circuit for processing light information based on such detected value, enable a stable read of light information and a simplified design of a signal processing circuit at the following stage.

Claims

1. A photoelectric conversion cell comprising a semiconductor transistor having a first emitter (5), a collector (3, 1, 11), and a base (4), and the transistor further having a first emitter electrode (8) connected to the first emitter (5) and isolated from the base (4), and a control electrode (7) capacitively coupled to the base (4),

charges being stored in the base (4) in response to incident light, and potentials being applied to the control electrode (7) so that in a read operation a first output signal, read from the first emitter (5) via the first emitter electrode (8) during or after an operation of storing charges in the base (4), is controlled by the level of charges stored in the base (4) and in a refresh operation the level of charges stored in the base (4) is restored to an initial level,

in which the transistor has a second emitter (5'), formed in the base (4) and separate from the first emitter (5) and having the same conductivity type as the first emitter (5), and a second emitter electrode (8') is connected to the second emitter (5') and isolated from the base (4), whereby a second output signal read from the second emitter (5') via the second emitter electrode (8') during or after the operation of storing charges in the base is also controlled by the level of charges stored in the base (4).

2. A photoelectric conversion device comprising a plurality of cells according to claim 1, a read-out circuit (21, 28, 31-35, 39-44), and a control circuit (45, 48), the read-out circuit (21, 28, 31-35, 39-44) reading out the first output signals from the cells under the control of the control circuit (45, 48), and the control circuit (45, 48) being coupled to the second emitters (5') of the cells to receive a control output signal therefrom and controlling the read-out circuit in accordance with the control output signal.

3. A photoelectric conversion device according to claim 2, wherein said carriers are accumulated in said bases (4) during an accumulation time and said control circuit (48) is operable to effect said control by varying said accumulation time.

4. A photoelectric conversion device according to claim 3, wherein the control circuit (48) is coupled to the second emitters (5') to receive the control output signal during the accumulation period.

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Each emitter electrode 8 takes a voltage of each light information of the photoelectric conversion cells 20-1 to 20-n because the transistors 28-1 to 28-n and 25-1 to 25-n are being OFF. Contrary to this, each emitter electrode 8' takes a peak voltage Vpk among those light information because the emitter electrode 8' is connected to the common line 22.

A change in the peak voltage Vpk is detected by the control circuit 48. When the peak voltage Vpk reaches a preset voltage V_0 (time t_4), the control circiut 48 makes the signal ϕ_t high level and makes the transistors 28-1 to 28-n turn ON. Then, the store operation terminates where light information appearing at the vertical lines 21-1 to 21-n is stored in the charge store capacitors 31-1 to 31-n. The following operation (after time t_5) for sequentially outputting light information stored in the charge store capacitors 31-1 to 31-n, is similar to that of the first example shown in Fig. 3B.

In the second example of the image pickup device, a peak voltage Vpk is detected from the emitter electrode 8', and the period of a store operation is controlled based on the peak voltage Vpk. Therefore, similar to the first example, it is possible to suppress the signal quantity difference between high and low level light signals and realize an automatic stop function. It is obvious that the second example can be applied to the first example to regulate the amplification factor of the amplifier 43 based on the peak voltage Vpk.

In the above embodiment, although the photoelectric conversion cells have been disposed one-dimensionally as a line sensor, obviously the present invention is also applicable to an area sensor having cells disposed two-dimensionally.

As seen from the foregoing description, the photoelectric conversion device according to the present invention can read light information from a semiconductor region provided separately from the electrode region. Therefore, light information can be read from the main electrode region and also from the semiconductor region. Thus, semiconductor region can be used, for example, in measuring the incident light quantity or detecting a peak value. Consequently, the measuring the incident light quantity or detecting a peak value can be carried out in parallel with such as a store operation or a read operation, resulting in a high speed operation of the device. Further, use of a circuit for processing light information based on such detected value, enable a stable read of light information and a simplified design of a signal processing circuit at the following stage.

Claims

1. A photoelectric conversion cell comprising a semiconductor transistor having a first emitter (5), a collector (3, 1, 11), and a base (4), and the transistor further having a first emitter electrode (8) connected to the first emitter (5) and isolated from the base (4), and a control electrode (7) capacitively coupled to the base (4),

charges being stored in the base (4) in response to incident light, and potentials being applied to the control electrode (7) so that in a read operation a first output signal, read from the first emitter (5) via the first emitter electrode (8) during or after an operation of storing charges in the base (4), is controlled by the level of charges stored in the base (4) and in a refresh operation the level of charges stored in the base (4) is restored to an initial level,

in which the transistor has a second emitter (5'), formed in the base (4) and separate from the first emitter (5) and having the same conductivity type as the first emitter (5), and a second emitter electrode (8') is connected to the second emitter (5') and isolated from the base (4), whereby a second output signal read from the second emitter (5') via the second emitter electrode (8') during or after the operation of storing charges in the base is also controlled by the level of charges stored in the base (4).

2. A photoelectric conversion device comprising a plurality of cells according to claim 1, a read-out circuit (21, 28, 31-35, 39-44), and a control circuit (45, 48), the read-out circuit (21, 28, 31-35, 39-44) reading out the first output signals from the cells under the control of the control circuit (45, 48), and the control circuit (45, 48) being coupled to the second emitters (5') of the cells to receive a control output signal therefrom and controlling the read-out circuit in accordance with the control output signal.

3. A photoelectric conversion device according to claim 2, wherein said carriers are accumulated in said bases (4) during an accumulation time and said control circuit (48) is operable to effect said control by varying said accumulation time.

4. A photoelectric conversion device according to claim 3, wherein the control circuit (48) is coupled to the second emitters (5') to receive the control output signal during the accumulation period.

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5. A photoelectric conversion device according to claim 2, wherein said control circuit (45) comprises gain control means for adjusting the gain of said first output signals.

6. A photoelectric conversion device according to any one of claims 2 to 5, in which the second emitters (5') are coupled to the control circuit through a common input line (22).

7. A photoelectric conversion device according to any one of claims 2 to 6, in which the control output signal is the greatest said second output signal.

8. A photoelectric conversion device according to any one of claims 2 to 6, in which in the refresh operation to restore the level of charges stored in the bases (4) to an initial level, current flows between the bases (4) and a circuit portion external to the transistors via both of the respective first emitters (5) and the respective second emitters (5').

9. A photoelectric conversion device according to any one of claims 2 to 8, in which the bases (4) receive signals from respective control electrodes (7) which are coupled to a common signal input line (23).

10. A photoelectric conversion device according to any one of claims 2 to 9, in which the read-out circuit comprises respective switches (28) coupled to the first emitters (5) of respective said transistors (20), the switches (28) receiving switch control signals (ϕt) over a common signal line (29).

11. A photoelectric conversion device according to claim 10, in which the read-out circuit further comprises respective signal storage means (31) coupled to the respective switches (28) on the side remote from the transistors (20).

12. A photoelectric conversion device according to claim 11, in which the read-out circuit comprises respective further switches (34) each coupled on one side to a respective said signal storage means (31), and each coupled on the other side to a common output line (35).

13. A photoelectric conversion device according to claim 12, in which the read-out circuit comprises means (32) to control the further switches (34) to connect the signal storage means (31) to the common output line (35) sequentially.

14. A photoelectric conversion device according to any one of claims 2 to 9, in which the read-out circuit comprises switches (34) provide output signals derived from respective said transistors (20) sequentially.

Patentansprüche

1. Lichtelektrische Wandlerzelle, die einen Halbleitertransistor mit einem ersten Emitter (5), einem Kollektor (3, 1, 11) und einer Basis (4) aufweist, wobei der Transistor des weiteren mit einer mit dem ersten Emitter (5) verbundenen und von der Basis (4) entkoppelten ersten Emitterelektrode (8) und mit einer kapazitiv an die Basis (4) gekoppelten Steuerelektrode (7) versehen ist,

   wobei in der Basis (4) Ladungen abhängig vom einfallenden Licht gespeichert und an der Steuerelektrode (7) Potentiale angelegt werden, so daß in einem Lesevorgang ein aus dem ersten Emitter (5) über die erste Emitterelektrode (8) bei oder nach einem Ladungsspeichervorgang in der Basis (4) gelesenes erstes Ausgangssignal von der Menge der in der Basis (4) gespeicherten Ladungen gesteuert wird, und in einem Auffrischungsvorgang die Menge der in der Basis gespeicherten Ladungen auf einen Ausgangswert zurückgeführt wird,

   ferner der Transistor einen in die Basis (4) eingeformten und vom ersten Emitter (5) getrennten zweiten Emitter (5') vom gleichen Leitfähigkeitstyp wie der erste Emitter (5) sowie eine zweite Emitterelektrode (8') aufweist, die mit dem zweiten Emitter (5') verbunden und von der Basis (4) entkoppelt ist, wobei ein vom zweiten Emitter (5') bei oder nach dem Ladungsspeichervorgang in der Basis über die zweite Emitterelektrode (8') gelesenes zweites Ausgangssignal ebenfalls von der Menge der in der Basis (4) gespeicherten Ladungen gesteuert wird.

2. Lichtelektrische Wandleranordnung mit einer Vielzahl von Zellen gemäß Anspruch 1, einer Ausleseschaltung (21, 28, 31 bis 35, 39 bis 44) und einer Steuerschaltung (45, 48), wobei die Ausleseschaltung (21, 28, 31 bis 35, 39 bis 44) die ersten Ausgangssignale aus den Zellen von der Steuerschaltung (45, 48) gesteuert ausliest, und wobei die Steuerschaltung (45, 48) an die zweiten Emitter (5') der Zellen gekoppelt ist, um von dort ein Steuerausgangssignal zu empfangen und die Ausleseschaltung entsprechend dem Steuerausgangssignal zu steuern.

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3. Lichtelektrische Wandleranordnung nach Anspruch 2, in der die Ladungen innerhalb einer Akkumulierzeit in den Basen (4) gesammelt werden, und in der die Steuerschaltung (48) in der Lage ist, die Steuerung durch Variieren der Akkumulierzeit zu bewirken.

4. Lichtelektrische Wandleranordnung nach Anspruch 3, in der die Steuerschaltung (48) an die zweiten Emitter (5') angekoppelt ist, um das Steuerausgangssignal innerhalb der Akkumulierzeit zu empfangen.

5. Lichtelektrische Wandleranordnung nach Anspruch 2, in der die Steuerschaltung (45) Verstärkungsregelmittel zum Einstellen der Verstärkung der ersten Ausgangssignale aufweist.

6. Lichtelektrische Wandleranordnung nach einem der Ansprüche 2 bis 5, in der die zweiten Emitter (5') über eine gemeinsame Eingangsleitung (22) an die Steuerschaltung gekoppelt sind.

7. Lichtelektrische Wandleranordnung nach einem der Ansprüche 2 bis 6, in der das Steuerausgangssignal das größte zweite Ausgangssignal ist.

8. Lichtelektrische Wandleranordnung nach einem der Ansprüche 2 bis 6, in der in dem Auffrischungsvorgang, bei dem die Menge der in den Basen (4) gespeicherten Ladungen auf den Ausgangswert zurückgeführt wird, Strom zwischen den Basen (4) und einem Schaltungsabschnitt außerhalb der Transistoren sowohl über die entsprechenden ersten Emitter (5) als auch über die entsprechenden zweiten Emitter (5') fließt.

9. Lichtelektrische Wandleranordnung nach einem der Ansprüche 2 bis 8, in der die Basen (4) aus den entsprechenden, an eine gemeinsame Signalleitung (23) gekoppelten Steuerelektroden (7) Signale empfangen.

10. Lichtelektrische Wandleranordnung nach einem der Ansprüche 2 bis 9, in der die Ausleseschaltung Schalter (28) aufweist, die an die ersten Emitter (5) der entsprechenden Transistoren (20) gekoppelt sind, wobei die Schalter (28) über eine gemeinsame Signalleitung (29) Schaltsteuersignale (ϕt) empfangen.

11. Lichtelektrische Wandleranordnung nach Anspruch 10, in der die Ausleseschaltung des weiteren Signalspeichermittel (31) enthält, die jeweils an die den Transistoren abgewandte Seite der entsprechenden Schalter (28) gekoppelt sind.

12. Lichtelektrische Wandleranordnung nach Anspruch 11, in der die Ausleseschaltung weitere Schalter (34) enthält, die jeweils an einer Seite an eines der Signalspeichermittel (31) und jeweils an der anderen Seite an eine gemeinsame Ausgangsleitung (35) gekoppelt sind.

13. Lichtelektrische Wandleranordnung nach Anspruch 12, in der die Ausleseschaltung Mittel (32) aufweist, die die weiteren Schalter (34) zur aufeinanderfolgenden Ankopplung der Signalspeichermittel (31) an die gemeinsame Ausgangsleitung (35) steuern.

14. Lichtelektrische Wandleranordnung nach einem der Ansprüche 2 bis 9, in der die Ausleseschaltung Schalter (34) zur sequentiellen Ableitung der Ausgangssignale aus den zugehörigen Transistoren (20) aufweist.

Revendications

1. Cellule de conversion photoélectrique comportant un transistor à semiconducteur ayant un premier émetteur (5), un collecteur (3, 1, 11) et une base (4), le transistor ayant en outre une électrode (8) de premier émetteur connectée au premier émetteur (5) et isolée de la base (4), et une électrode (7) de commande en couplage capacitif avec la base (4),

des charges étant emmagasinées dans la base (4) en réponse à une lumière incidente, et des potentiels étant appliqués à l'électrode (7) de commande afin que, dans une opération de lecture, un premier signal de sortie, lu sur le premier émetteur (5) par l'intermédiaire de l'électrode (8) de premier émetteur pendant ou après une opération d'emmagasinage de charges dans la base (4), soit commandé par le niveau de charges emmagasinées dans la base (4) et que, dans une opération de régénération, le niveau de charges emmagasinées dans la base (4) soit rétabli à un niveau initial,

le transistor comportant un second émetteur (5'), formé dans la base (4) et séparé du premier émetteur (5) et ayant le même type de conductivité que le premier émetteur (5), et une électrode (8') de second émetteur connectée au second émetteur (5') et isolée de la base (4), grâce à quoi un second signal de sortie, lu sur le second émetteur (5') par l'intermédiaire de l'électrode (8') de second émetteur, pendant ou après l'opération d'emmagasinage de charges dans la base, est également commandé par le niveau de charges emmaga-

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sinées dans la base (4).

2. Dispositif de conversion photoélectrique comprenant plusieurs cellules selon la revendication 1, un circuit d'extraction (21, 28, 31-35, 39-44), et un circuit de commande (45, 48), le circuit d'extraction (21, 28, 31-35, 39-44) extrayant les premiers signaux de sortie des cellules sous la commande du circuit de commande (45, 48), et le circuit de commande (45, 48) étant couplé aux seconds émetteurs (5') des cellules afin d'en recevoir un signal de sortie de commande et commandant le circuit d'extraction conformément au signal de sortie de commande.

3. Dispositif de conversion phooélectrique selon la revendication 2, dans lequel lesdits porteurs sont accumulés dans lesdites bases (4) durant un temps d'accumulation et ledit circuit de commande (48) peut fonctionner de façon à effectuer ladite commande par variation dudit temps d'accumulation.

4. Dispositif de conversion photoélectrique selon la revendication 3, dans lequel le circuit de commande (48) est couplé aux seconds émetteurs (5') afin de recevoir le signal de sortie de commande durant la période d'accumulation.

5. Dispositif de conversion photoélectrique selon la revendication 2, dans lequel ledit circuit de commande(45) comprend un moyen de commande de gain destiné à régler le gain desdits premiers signaux de sortie.

6. Dispositif de conversion photoélectrique selon l'une quelconque des revendications 2 à 5, dans lequel les seconds émetteurs (5') sont couplés au circuit de commande par une ligne d'entrée commune (22).

7. Dispositif de cnversion photoélectrique selon l'une quelconque des revendications 2 à 6, dans lequel le signal de sortie de commande est le plus grand second signal de sortie.

8. Dispositif de conversion photoélectrique selon l'une quelconque des revendications 2 à 6, dans lequel, dans l'opération de régénération pour établir le niveau de charges emmagasinées dans les bases (4) à un niveau initial, un courant circule entre les bases (4) et une partie de circuit extérieure aux transistors en passant à la fois par les premiers émetteurs respectifs (5) et les seconds émetteurs respectifs (5').

9. Dispositif de conversion photoélectrique selon l'une quelconque des revendications 2 à 8, dans lequel les bases (4) reçoivent des signaux provenant d'électrodes de commande respectives (7) qui sont couplées à une ligne commune (23) d'entrée de signaux.

10. Dispositif de conversion photoélectrique selon l'une quelconque des revendications 2 à 9, dans lequel le circuit d'extraction comprend des commutateurs respectifs (28) couplés aux premiers émetteurs (5) desdits transistors respectifs (20), les commutateurs (28) recevant des signaux (ϕ_t) de commande de commutateurs par une ligne commune (29) de signaux.

11. Dispositif de conversion photoélectrique selon la revendication 10, dans lequel le circuit d'extraction comporte en outre des moyens respectifs (31) de stockage de signaux couplés aux commutateurs respectifs (28) sur le côté éloigné des transistors (20).

12. Dispositif de conversion photoélectrique selon la revendication 11, dans lequel le circuit d'extraction comporte d'autres commutateurs respectifs (34) couplés chacun, sur un côté, à l'un, respectif, desdits moyens (31) de stockage de signaux, et couplés chacun, sur l'autre côté, à une ligne commune (35) de sortie.

13. Dispositif de conversion photoélectrique selon la revendication 12, dans lequel le circuit d'extraction comporte des moyens (32) destinés à commander les autres commutateurs (34) pour connecter séquentiellement les moyens (31) de sockage de signaux à la ligne commune (35) de sortie.

14. Dispositif de conversion photoélectrique selon l'une quelconque des revendications 2 à 9, dans lequel le circuit d'extraction comporte des commutateurs (34) destinés à produire des signaux de sortie provenant séquentiellement desdits transistors respectifs (20).