Method and Process Using Fingerprint Based Semiconductor Manufacturing Process Fault Detection

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit of and priority to U.S. Patent Application No. 17/484,204, filed September 24, 2021, and entitled "Method and Process Using Fingerprint Based Semiconductor Manufacturing Process Fault Detection", the contents of which are incorporated by reference in their entirety for all purposes.

BACKGROUND

[0002] The present disclosure relates to the processing of substrates. In one embodiment, this disclosure provides a novel method for the processing of substrates used to form microelectronic devices.

[0003] A microelectronic device is an individual electronic device and component or a collection thereof at a micrometer or smaller scale. An individual microelectronic device may include electronic components, such as transistors, capacitors, inductors, resistors, diodes, and the like, which may be connected to form combinations in accordance with a design. The connections may be formed by integrating a multi-layer interconnect network of vertical and lateral conductors isolated by insulators. The combinations may form electronic circuitry that collectively perform complex functions such as data storage and retrieval, computation, signal processing, and electronic image capture, or combinations thereof. An integrated circuit (IC), sometimes called a microchip, is an example of such a device. IC's are used in many electronic systems for industrial, military, and consumer applications.

[0004] Typically, the microelectronic devices are formed on a substrate (such as for example a semiconductor wafer) and produced as part of a stack of patterned layers of materials, e.g., semiconductors, insulators, and conductors on the substrate. Typically, substrate processing involves a series of process steps using a variety of process tools to form, implant, treat, pattern, etch, etc. a variety of process layers through the sequenced use of a wide variety of process tools. With innovations in

processing technology, the minimum feature sizes have been periodically reduced to increase the packing density of components in a microelectronic device. With more components, the functionality of electronic circuits has been enhanced, thereby enabling a microelectronic device to perform more complex tasks.

[0005] As the complexity of substrate processing increases with increasing numbers of electronic components in each microelectronic device and geometries in substrate processing continue to shrink, the technical challenges to forming structures on substrates have increased. Innovations in semiconductor wafer fabrication manufacturing systems, manufacturing methods and manufacturing tools may be needed to provide low cost electrical-mechanically functional microelectronic devices produced by high yield semiconductor fabrication methods.

[0006] The increased complexity and decreased geometries of substrate processing also requires more precise manufacturing tools and control of those manufacturing tools. Faulty tool parts can lead to poor performance of devices formed by the substrate processing. Early detection of faulty parts can save costs and prevent catastrophic failure. Traditional ways to detect faulty parts is to examine the processed wafer by setting a uniform threshold or installing sensors that detect abnormalities in the machine.

[0007] It would be desirable to provide an improved technique for monitoring and controlling the various process steps and process tools utilized in substrate processing.

SUMMARY

[0008] Sensitivity calculations of a process model through the rate of change of a model fingerprint with respect to process variables are provided. A table of fingerprint sensitivities is generated, where process variables are associated with a set of fingerprint sensitivity. The fingerprint of incoming substrates is monitored through a production process by applying the same fingerprint method that is used in the process model. Calculations are made of the difference between the incoming substrate fingerprint and the predicted fingerprint which is calculated using the process model. This difference fingerprint is compared against the table of fingerprint sensitivities to find the process variable most likely to be responsible for the

difference. A chart that ranks this likelihood may then be created and reported to the user. Spatial relationships between process variables and actual measurements on the substrate may be obtained. Direct correlation through fingerprint sensitivity improves the ability to pinpoint faulty process tools. In another alternative, the fingerprint process may be utilized to detect defects which have formed on the substrate. For example, particulates that may form on a substrate at a particular process step may be detected through use of the fingerprint comparison process described herein.

[0009] Faulty process tools (or parts of the process tool) may have significant impact on the fingerprint of the processed substrate. Similarly defects may have significant impact on the fingerprint of the processed substrate. The disclosed methods present the detail of using fingerprint modeling to detect process variable related drifts to identify faulty process tools and/or parts early and/or to detect the formation of defects at a process step. The technique disclosed does not require sensor input to detect faulty tools and/or defects. Thus, an alternative method to identify root causes of a substrate processing process problem or faulty tools and/or parts by isolating process variables with contributing fingerprint components and detection based on the process variable sensitivity is provided. Similarly, the disclosed methods present the detail of using fingerprint modeling to detect the formation of defects at a process step. The technique disclosed does not require sensor input to the defects. Thus, an alternative method to identify a substrate processing problems forming defects by use of fingerprint techniques is provided.

[0010] In one embodiment, a method is provided for characterizing a fabrication process for manufacturing a semiconductor wafer, the fabrication process comprising at least one process step, the at least one process step being associated with a plurality of process variables. The method comprises performing a design of experiment process for the at least one process step, wherein the plurality of process variables are changed for a plurality of design of experiment semiconductor wafers; obtaining design of experiment wafer measurements of a first characteristic from the plurality of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the measurement is obtained;

creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints; creating a process model of the at least one process step utilizing the plurality of design of experiment process step fingerprints; performing the at least one process step on a production semiconductor wafer; obtaining production wafer measurements of the first characteristic of the production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the production semiconductor wafer from which the measurement is obtained; creating a production semiconductor wafer process step fingerprint from the obtained production semiconductor wafer measurements; and detecting a faulty process variable of the at least one process step utilizing the production semiconductor wafer process step fingerprint and the process model.

[0011] The method may further comprises calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of the at least one process step.

[0012] The method may also comprise calculating a difference between the modeled fingerprint and the production semiconductor wafer process step fingerprint; and utilizing the calculated difference when detecting the faulty process variable of the at least one process step. In one embodiment, the faulty process variable is detected by comparing the calculated difference against a process model sensitivity to help determine if a particular process variable is faulty. In one embodiment, the particular process variable is identified utilizing a probability determination. In one embodiment, the particular process variable is identified by analyzing a plurality of process model terms obtained by comparing the calculated difference against the process model sensitivity, to identify a process variable exceeding a predetermined fault probability level.

[0013] Another method is a method of characterizing a fabrication process for manufacturing a semiconductor wafer, the fabrication process comprising a plurality of process steps, at least a first one of the plurality of process steps being associated with a plurality of process variables. The method may comprise performing a design of experiment process. The design of experiment process may comprise for a series

of design of experiment semiconductor wafers, performing the first one of the plurality of process steps on the series of design of experiment semiconductor wafers, wherein at least one or more of values of the plurality of process variables are changed for each of the series of design of experiment semiconductor wafers; obtaining design of experiment wafer measurements of a first characteristic from the series of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the design of experiment wafer measurement is obtained; creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints; and creating a process model of the first one of the plurality of process steps utilizing the plurality of design of experiment process step fingerprints. The method further comprises performing the first one of the plurality of process steps on at least one production semiconductor wafer; obtaining production wafer measurements of the first characteristic of the production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the production semiconductor wafer from which the measurement is obtained; creating a production wafer process step fingerprint from the obtained production wafer measurements; and detecting a faulty process variable utilizing the production wafer process step fingerprint and the process model.

[0014] The method may further comprise calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of the first one of the plurality of process steps. The method may also comprise calculating a difference between the modeled fingerprint and the production wafer process step fingerprint. The method may also comprise calculating a difference between the modeled fingerprint and the production wafer process step fingerprint; and utilizing the calculated difference when detecting the faulty process variable of the first one of the plurality of process steps. In some embodiments, the faulty process variable is detected by comparing the calculated difference against variable sensitivity levels of the process model to help determine that a particular process variable is the faulty process variable. In some embodiments, the faulty process variable is identified utilizing a probability determination. In some embodiments, the faulty process

variable is identified by analyzing a plurality of process model terms obtained by comparing the calculated difference against the variable sensitivity levels, to identify a process variable exceeding a predetermined fault probability level. In other embodiments, the faulty process variable is identified utilizing a probability determination.

[0015] In another embodiment, a method is provided for characterizing a fabrication process for manufacturing a semiconductor wafers, the fabrication process comprising a plurality of process steps, at least a first one of the plurality of process steps being associated with a plurality of process variables. The method may comprise performing a design of experiment process, the design of experiment process comprising: for a series of design of experiment semiconductor wafers, performing the first one of the plurality of process steps on the series of design of experiment semiconductor wafers, wherein at least one or more of values of the plurality of process variables are changed for each of the series of design of experiment semiconductor wafers; obtaining design of experiment wafer measurements of a first characteristic from the series of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the design of experiment measurement is obtained; creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints; and creating a process model of the first one of the plurality of process steps utilizing the from the plurality of design of experiment process step fingerprints. The method also comprises performing the first one of the plurality of process steps on at least one production semiconductor wafer; obtaining production wafer measurements of the first characteristic of the at least one production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the at least one production semiconductor wafer from which the measurement is obtained; calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of first one of the plurality of process steps; and detecting a defect on the at least one production semiconductor wafer utilizing the calculated modeled fingerprint for the at least one production semiconductor wafer and the process

model, wherein the process model is utilized to account for process variable variations so as to improve the defect detection accuracy.

[0016] In some embodiments, the defect on the at least one production semiconductor wafer is determined by identifying spatially localized abnormalities and considering process variable variations to eliminate false detections of defects. The method may further comprise calculating a difference between the obtained production wafer measurements and the calculated modeled fingerprint. The method may also comprise calculating a difference between obtained production wafer measurements and the calculated modeled fingerprint; and utilizing the calculated difference when detecting the defect on the at least one production semiconductor wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] A more complete understanding of the present inventions and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features. It is to be noted, however, that the accompanying drawings illustrate only exemplary embodiments of the disclosed concepts and are therefore not to be considered limiting of the scope, for the disclosed concepts may admit to other equally effective embodiments.

[0018] Figure 1A illustrates an example of a measurable outcome of a process step of a wafer fabrication manufacturing system, in accordance with one embodiment.

[0019] Figures 1B and 1C illustrate an example fingerprint of the measurable outcome illustrated in Figure 1A.

[0020] Figure 2 is a flowchart illustrating a portion of an example method in a wafer fabrication manufacturing system used for generating fingerprint models, transfer functions, and process model of a process step from in-line measurements of wafer fabrication metrology, in accordance with one embodiment.

[0021] Figures 3A-3C illustrate a portion of an example method wherein a measurement fingerprint of an in-line measurement type is generated, in accordance with one embodiment.

[0022] Figures 4A-4D illustrate a portion of an example method wherein a process model of a measurement fingerprint of an in-line measurement type is generated, in accordance with one embodiment.

[0023] Figure 5 is a flowchart illustrating a portion of an example method in a wafer fabrication manufacturing system used for generating fingerprint models, transfer functions, and process model of a process module from in-line measurements of wafer fabrication metrology, in accordance with one embodiment.

[0024] Figure 6A-6C illustrate an example method of generating a hierarchy of fingerprints from measurement fingerprints, in accordance with one embodiment.

[0025] Figure 7 is a generalized flowchart illustrating an example method of generating a model for a baseline process flow, in accordance with one embodiment.

[0026] Figure 8 illustrates an exemplary work flow diagram for implementing a fingerprint based fault detection technique for use with semiconductor wafers.

[0027] Figure 9 illustrates an exemplary table illustrating a variety of process variables for a film formation process.

[0028] Figure 10 illustrates the film thickness raw data spatially collected across a grid of a monitor wafer and the corresponding coefficient strength and coefficients as provided by the fingerprint model.

[0029] Figures 11A and 11B illustrate some of the work flow steps of Figure 8 with regard to the film thickness example for “good” and “bad” wafer.

[0030] Figures 12A and 12B illustrate charts plotting the process variable (process model term) against the probability of fault for a “good” and “bad” wafer.

[0031] Figure 13 illustrates an exemplary work flow diagram for implementing a fingerprint based defect detection technique for use with semiconductor wafers.

[0032] Figures 14-16 illustrate exemplary methods utilizing techniques disclosed herein.

DETAILED DESCRIPTION

[0033] Existing approaches for the fabrication of substrates such as semiconductor wafers use metrics that are a single value that is applied to or assumed to apply across the entire substrates. The conventional applications of these metrics are based on measurements of an individual or sample substrate.

[0034] These conventional approaches discard or ignore information related to or associated with each measurement. For example, such information may include spatial or correlations between measurements. Such information is potentially valuable. Edge Placement Error (EPE) is an example of a combination of different measurements to form a metric that can be correlated to yield.

[0035] Pending U.S. Patent Application No. 16/666,087 filed October 28, 2019, entitled Systems and Methods for Manufacturing Microelectronic Devices by Fonseca and Ip, (the disclosure of which is expressly incorporated by reference in its entirety) describes manufacturing systems which adopt methods wherein fingerprints (FP's) of metrics that correlate to manufacturing yield are generated from one or more in-line measurements performed at multiple spatial locations of one or more semiconductor wafers.

[0036] The technology described in the incorporated by reference U.S. Patent Application No. 16/666,087, in various embodiments, preserves spatial information by generating a process model built using a lot more available information. In addition, the technology, in various embodiments, can be dynamically applied to semiconductor manufacturing and is amenable to be automated using a feedback control loop.

[0037] Embodiments of semiconductor wafer fabrication manufacturing systems manufacturing methods, and manufacturing tools described herein may improve manufacturing yield and manufacturing cost of microelectronic devices produced by the technique of semiconductor wafer fabrication. Semiconductor wafer fabrication may be described as execution of a sequence of process modules; each process

module comprising a series of unit process steps. Example unit process steps include surface preparation, ion implantation, thermal steps (e.g., rapid thermal oxidation (RTO), rapid thermal anneal (RTA), and laser anneal), photolithography steps (e.g., resist coat, exposure, develop, and strip), electroplating, plasma deposition, plasma etch, wet etch, chemical mechanical polish (CMP), and the like, performed in accordance with a sequential process flow to fabricate a layer, for example, an active layer, dummy gate layer, source-drain layer, metal gate layer, contact layer, and the like. The respective process modules may be referred to as the active module, dummy gate module, and so on. The manufacturing yield of a semiconductor wafer production line may be considered to be the fraction of the completed microelectronic devices having electrically testable metrics (e.g., transistor leakage, resistor resistance, circuit functionality, etc.) that conform to a set of specifications.

[0038] Fingerprints (FP's) of metrics that correlate to manufacturing yield are generated from one or more in-line measurements performed at multiple spatial locations of one or more semiconductor wafers. For each layer, FP's of metrics appropriate for the layer are generated, as described in further detail below. For example, an FP for edge placement error (EPE) may be generated for the dummy gate layer. In some embodiments, each FP is a mathematical model of the respective metric that retains the spatial information of the measurements. In some embodiments, the mathematical model is a mathematical function of the spatial coordinates of the locations on a wafer from where the in-line measurements have been obtained. The mathematical function may be expanded in a finite series of mathematical functions, referred to as basis functions. The FP may then be represented by a coefficient vector comprising an ordered set of the coefficients of respective terms of the series expansion of the model function. As described in further detail below, the FP of a layer metric may be a composite of a hierarchy of FP's. For example, the active layer EPE FP may be a composite mathematical model including contributions from several FP's such as height of mandrel (used for sidewall image transfer (SIT)), pitch-walk (for multiple patterning techniques), overlay (e.g., alignment errors between an active mask and an alignment mask), and the like. These FP's (e.g., mandrel height, pitch-walk, and overlay) may, in turn, be derived from one or more FP's of, e.g., in-line measurements such as deposited film

thickness of the mandrel, pitch of multiple patterns of a sidewall hard mask, dimensions of features in an overlay pattern, and the like.

[0039] The in-line measurements are designed to identify outcomes of the preceding process steps that may eventually impact the manufacturing yield at the end of the wafer fabrication production line. As known to persons skilled in the art, an outcome of processing steps may be modulated by a set of adjustable process parameters. The process parameters are generally equipment settings selected to execute one or more process steps. For example, a dummy gate resist EPE measurement after a resist develop process step in the dummy gate process module may be modulated by a wafer spin speed at a resist coat step, and an exposure time and a position of a focal plane during a photoresist exposure step. Accordingly, each coefficient of the FP for the dummy gate resist EPE may be modulated by the adjustable process parameters: in this example, the spin speed, exposure, and focus. The response of an FP coefficient (e.g., the dummy gate resist EPE FP) to a set of process parameters (e.g., spin speed, exposure, and focus) may be modeled as a mathematical function of a set of independent variables, wherein each variable is a numerical representation of a process parameter appropriately normalized to the units for EPE (e.g., nanometer). These mathematical descriptions collectively form a process model for the dummy gate resist EPE.

[0040] In this example, because the dummy gate resist EPE is a direct measurement, its FP is one of the bottom level FP's in the hierarchy of FP's. It may be further noted, that in this embodiment, the process model may retain the spatial information in the dummy gate resist EPE measurements by accurately modeling the dummy gate resist EPE FP. In general, there may be more than one measurement type, (e.g., EPE, line edge roughness (LER), overlay, critical dimension (CD), linewidth roughness (LWR), and the like). A bottom level FP having its respective process model may be generated for each measurement type of the process step. Combinations and calculations (e.g., the difference between two measurements) with the in-line measurement FP's for measurements obtained at the present or previous process steps may be done to create a next higher level of FP's for that process step.

[0041] The measurable outcomes of a process step often depend on the state of the incoming wafer. For example, EPE of the dummy gate resist pattern may be affected by the height of fins formed protruding above shallow trench isolation (STI) oxide at the active level in a process flow comprising fabrication of a fin-shaped transistor structure called FinFET. The fin-heights measured in the active process module may be accurately reproduced by an active fin-height FP. The state of the incoming wafer is generally determined both by the previous process modules and by the completed process steps of the current process module. Accordingly, the top level FP's of the previous process modules and the highest level FP's of the completed steps in the present process module may correlate to measurements at a subsequent process step; hence correlate to the FP's generated therefrom. In this example, the active fin-height FP may influence one or more FP's of in-line measurements at the dummy gate layer, such as the dummy gate resist FP's for EPE, CD, LER, LWR, and overlay. Such correlations between pairs of FP's (e.g., between the active fin-height FP and the dummy gate resist EPE FP) are characterized for the process flow and fed forward from the previous process steps as transfer functions suitable for use in generating the measurement (bottom level) FP's of the subsequent process step. In one embodiment, a transfer function may be implemented as a transformation matrix that maps a coefficient vector of an earlier FP (e.g., the active fin-height FP) to a component vector that can be incorporated in the coefficient vector of a bottom level FP of the subsequent process step (e.g., the dummy gate resist EPE FP). In general, a transfer function may be implemented using any numerical model such as, a transformation matrix, a set of differential equations, a look-up table, a set of statistical correlation functions, or an iterative algorithm, or the like that may be used to include the impact of a metric computed from wafer characteristics of previous process steps on the FP of a metric derived from measurements done at a subsequent process step. Furthermore, although we have formulated the influence of previous processing on the wafer characteristics at the immediate process step as a transfer function mapping one or more FP models at the previous process step on to at least a portion of a measurement FP at the immediate process step, other formulations are conceivable. For example, a transfer function may be formulated to describe a mapping of the process parameters at the previous step on to at least a portion of a FP model of a metric derived from a combination/calculation of one or more in-line wafer fabrication metrology data at the immediate process step. Once

the impact of the previous processing is incorporated into the bottom level FP, the correlations with previous process steps are naturally included in any higher level FP formed subsequently using the bottom level FP.

[0042] After generating the FP's for the process steps of a process module, combinations and calculations may be applied to generate the next higher level of FP's which could be the FP's of the process module or layer, as described further below. For example, several FP's of process steps in the dummy gate process module such as the dummy gate resist CD FP, the dummy gate etch bias FP, overlay, and others may be combined to generate a dummy gate CD FP for the dummy gate layer.

[0043] Embodiments of the method of using FP's and generating process models for the FP coefficients which retain and reproduce spatial coordinates of the raw measurement data is advantageous for monitoring and controlling a semiconductor wafer fabrication production line. A statistical process control (SPC) strategy employing a monitoring of the FP coefficient vectors that provide spatial information facilitates identifying the source of a process excursion that may be degrading the yield of a wafer fabrication production line. For example, if an increased radial dependence is observed from the abnormality in the coefficients in the FP of a metric that may be affected by several process parameters of which one represents a radial gas flow then that may suggest an abnormal gas flow. The process model for the FP coefficient showing an abnormal value could be utilized in conjunction with the spatial information to simulate the abnormality in order to help quickly identify the equipment and equipment setting where intervention may succeed in recovering the manufacturing yield.

[0044] Generating FP coefficient vectors wherein correlations with previous process steps are incorporated using transfer functions provides several unique advantages to a wafer fabrication manufacturing system. The transfer function method effectively partitions the coefficient vector of the measurement FP's into two component vectors: one that correlates with previous processing and another, referred to as the immediate step vector that correlates with the immediately completed process step. The component that correlates with fingerprints of earlier steps is predictable from the processing history and is referred to as the transferred vector or transferred

component of the measurement FP. Such a decomposition of the FP coefficient vector may be used to partition a deviation observed at a given process step into a portion due to the incoming wafer state and a portion due to the immediate process step. Furthermore, the predictability may be used to feed forward corrective actions or make early decisions on terminating further processing.

[0045] The transfer function method enhances the accuracy of the process model for the entire fabrication process flow by retaining the impact of all the earlier process steps in the FP for a metric in a subsequent process step. This capability may be advantageously used in computer aided analyses to adjust process parameters to improve the yield of the production line, as described in further detail below. The spatial information along with the process models may help in more targeted adjustments to optimize equipment settings to increase manufacturing yield. Furthermore, the analyses may identify specific equipment worth further investment because of its high impact on manufacturing yield, and may also identify specific equipment where a cheaper alternative may be used with negligible impact on the manufacturing yield.

[0046] The manufacturing systems and methods outlined above are illustrated in further detail below with reference to figures 1 through 8.

[0047] The wafer map in Figure 1A illustrates an example of a directly measurable outcome 100 of a process step (e.g., an EPE measurement of a resist patterning step) of a wafer fabrication manufacturing system, where the outcome is a collection of the same type of measurement repeated at multiple die locations on the wafer. A dataset comprising data values associated with a spatial location (e.g., two-dimensional (2D) rectangular coordinates, x and y, or polar coordinates r and □) on one sample wafer or a collection of such wafers may be displayed as a wafer map. In a wafer map each data point is given an area in a two-dimensional image of a wafer, in accordance with its associated spatial coordinates. In the wafer maps in this document, such as the image in Figure 1A, the data points are depicted as tessellated rectangles having values indicated by a grayscale.

[0048] The raw data (e.g., the directly measured EPE values and their associated coordinates) may be processed to create a fingerprint (FP) model. In particular, an

analysis, such as a regression analysis, may be performed to select and adjust the parameters of a function for a best fit to the raw data values, for example, the least error between the measured values of EPE and the values computed by an FP model using the optimized parameters. The analysis includes selecting an appropriate mathematical function of the 2D spatial coordinates that may reproduce the spatial patterns in the raw data with a manageable finite number of adjustable parameters. For example, measurements which may be sensitive to a process step where, for example, liquid photoresist is introduced in the center region of a spinning wafer and distributed across the wafer surface by radial centrifugal forces, the model function may be selected to be a function of the polar coordinates r and □□ expressed mathematically as a finite series of Zernike polynomials (or other functions such as Fourier series and Bessel functions). Each polynomial is weighted by its respective numerical coefficient. These coefficients are the fitting parameters of the model whose values may be optimized during the analysis to obtain the best fit to the raw data. An ordered set of coefficients is referred to as a coefficient vector, where each coefficient is one component of the coefficient vector. Collectively, the components (arranged in the same order as the order of the Zernike polynomials) constitute an FP model of the raw data. The coefficient vector illustrated in Figure 1B is an example of an FP model of the raw data depicted by the wafer map in Figure 1A. The model function used for the FP model in Figure 1B comprises a series of the first 21 Zernike polynomials weighted by 21 coefficients plotted in order in Figure 1B. The wafer map 120 in Figure 1C depicts the modeled values, as calculated using the optimized FP model illustrated in Figure 1B. As may be observed from a comparison of the two wafer maps (Figures 1A and 1C), the FP model in Figure 1B is able to reproduce the raw data fairly accurately.

[0049] In some instances, the initial FP model (e.g., the 21-dimensional coefficient vector in Figure 1B) may be simplified further by extending the analysis to include identifying the dominant model parameters. If the coefficient vector has few principal components (e.g., five coefficients that significantly affect the calculated data values) then the initial FP model comprising, for example, 21 coefficients, may be approximated by the few identified principal coefficients, for example, five principal coefficients. In some embodiments, the low-dimensional (e.g., five-dimensional) coefficient vector may replace the initial high-dimensional (e.g., 21-dimensional) FP

model for further processing and computation (the rest of the coefficients being ignored).

[0050] Figure 2 is a flowchart that illustrates an execution flow for one process step in an example system 200 that implements the techniques described above. The example system 200 is performed in cooperation with fabrication of semiconductor wafers. In some instances, the cooperation may include the example system 200 being an integral part of the fabrication itself. As described in detail below, processing steps in addition to the baseline (the plan-of-record) wafer fabrication process may be performed to obtain measurements to extract accurate model parameters with high confidence.

[0051] The example process is explained herein as being performed by a system 200 for simplicity sake and not any limitation. Figures 3 and 4 accompany the flowchart of Figure 2 to help explain some of the steps in system 200. Figure 3 is used to illustrate generation of a measurement FP as a function of the coordinates of measurement locations on the wafer. Figure 4 is used to explain the method using which system 200 generates a process model to compute the response of coefficients of the fingerprint models to changes in process parameters.

[0052] As indicated by block 210 in the flowchart of system 200 in Figure 2, the first step in the stepwise description of the method used in system 200 to create a predictive mathematical model of outcomes of a process step, the model comprising FP's, transfer functions, and process models, is to obtain in-line measurements of one or more characteristics (e.g., resist CD of lines in a pattern of dense lines) of semiconductor wafers processed in accordance with a baseline fabrication process flow. Each obtained measurement is associated with a wafer spatial location from which the measurement is obtained and may be depicted graphically by a wafer map, similar to that described with reference to Figure 1A. Graph 300 of Figure 3A is a wafer map of the raw data of measurements, for example, CD measurements gathered from a collection of baseline processed wafers, at the same set of locations on each wafer.

[0053] More generally, the actions of block 210 may be described as gathering in-line fabrication metrology data of the semiconductor wafers with spatial information of

that gathered data. This in-line fabrication metrology data is produced from in-line measurements taken of, about, on, in, and for the wafer of a characteristic that results from some process step of the baseline fabrication process flow. The measurement may be taken during the process step or after completion. That is, the in-line fabrication metrology data is a measurement of a characteristic of the wafer formed in the process step of the baseline semiconductor fabrication process flow.

[0054] In-line fabrication metrology data at a process step may be derived from measurements about a film of material processed in the process step (e.g., a deposited film thickness), patterns in the processed film (e.g., resist linewidth at resist develop step), devices completed by the processing at the process step (e.g., by metal CMP at an interconnect level), an inchoate device (e.g., an alignment mark) exposed by etching a material, and the like. Herein, the process step may be processing a material film that is the focus of the fabrication at that moment. Often, the film is the top or uppermost film. For example, the film is the one that is or was just deposited, cleaned, or etched.

[0055] In some instances, for example, the in-line fabrication metrology data may be derived from measurements about a film immediately adjacent the film that is the current focus of the fabrication, patterns in that adjacent layer, devices completed by the adjacent layer, an inchoate device exposed by the adjacent layer, and the like. Often, that immediate adjacent layer is the layer just below the uppermost film.

[0056] In still other instances, for example, the in-line fabrication metrology data may be derived from measurements about multiple adjacent layers of the wafer or of the wafer itself. For example, the multiple adjacent layers of the wafer may include electrically and/or mechanically interacting microelectronic devices therein.

[0057] Typically, the in-line fabrication metrology data includes measurements from (calculations based on measurements from) multiple semiconductor wafers using a common stack of patterns of materials during the semiconductor fabrication. Examples of different types of in-line fabrication metrology data include measuring and/or calculating data such as measuring and/or calculating in-line fabrication metrology data selected from a group consisting of EPE, grid CD measurements, block LWR measurements, grid LWR measurements, block CD measurements,

edge profile, selectivity for selective deposition and/or selective etch; electrical properties of the formed microelectronic devices; contact hole CD; contact hole edge roughness (CER) and ellipticity; tip-to-tip distances for short and long lines and trenches; overlay error measurements between two patterned layers; film thicknesses and thickness uniformities; measurements that occur after actions of a single tool; measurements that occur after all of the tools of a single process module; measurements that occur after multiple process modules; and a combination thereof.

[0058] At block 220, the system selects an appropriate mathematical function of the 2D spatial coordinates (x, y), or (r, □) to model the data. In one embodiment the model function is a finite series of basis functions and the numerical coefficients with which each term of the series is weighted is referred to as the coefficient vector or FP of the data, as explained above. The basis functions are generally orthogonal functions such as, Zernike polynomials, Legendre polynomials, or Bessel functions, or the like, and are chosen such that the in-line measurement type of interest may be accurately modeled without having to use a very long series requiring long computation times, and the characteristics of the model are comparable to some physical components of the in-line measurement step (e.g. radial characteristics of a spin coating process).

[0059] At the next block 230, the system 200 executes a computation that optimizes the finite set of coefficients for the best fit to the obtained spatial measurements of a measurement type to obtain the respective FP model, in accordance with an optimization algorithm. An FP model may be generated for each measurement type of in-line fabrication metrology data obtained at the process step. These measurement FP's are the first (lowest) level of FP's.

[0060] The in-line measurement and generation of the respective FP is illustrated in Figures 3A-3C. Figure 3A depicts in-line fabrication metrology raw data of a measurement type obtained from one or more wafers processed at the immediate process step using baseline processing. The graph displays the data as a wafer map of tessellated rectangles located at the spatial coordinates of the respective measurement type and shaded using a grayscale to represent a numerical value of the respective data. The data depicted in Figure 3A is then modeled using a finite

(e.g., 21-term) series of Zernike polynomials which are functions of the polar coordinates (r, □).

[0061] The optimized set of 21 coefficients is displayed as a histogram in Figure 3B, where the horizontal axis is the order of the Zernike polynomial and the vertical axis is the respective coefficient strength. In some embodiments, the number of terms may be adjustable, for example, higher order polynomials may be added to the series if the minimum fit error after optimization is higher than an acceptable threshold.

[0062] As seen in the histogram in Figure 3B, some of the coefficients are relatively small relative to others, indicating that it may be possible to simplify the model without introducing excessive fit error because the contribution of each term is proportional to the strength of its respective coefficient. However, it is important to also consider that the basis functions are functions of the 2D spatial coordinates and, therefore, the relative contribution of the terms also depend on the location on the surface of the wafer. For example, a term that is dominant near the center of the wafer may be weak near the edge of the wafer.

[0063] In Figure 3C, the contributions of five terms having the five highest coefficient strengths are plotted as 3-dimensional surfaces over the x-y plane of the wafer surface. As seen from the histogram in Figure 3B, the top five coefficients are those for the 4th, 12th, 10th, 21st, and 14th order Zernike polynomials. Graphs, such as those in Figure 3C help to reduce the complexity of the model. A less complex FP model provides the advantages of reducing computation time to generate process models and performing subsequent analysis, as described further below.

[0064] Next, at block 240 in this embodiment, transfer functions are obtained to decompose the measurement FP's at the current process step in order to model the influence of a previous process step on the outcome of in-line measurement of wafer characteristics obtained at the present process step. In another embodiment, the transfer functions may be generated after the generation of all the measurement FP's and higher level FP's (using combinations of measurement FP's and calculations) of the present process step is completed. As discussed above, the

transfer function may be implemented and extracted using various techniques, for example, transformation matrices, statistical correlation functions, etc.

[0065] As indicated in block 240 of the flowchart of system 200 in Figure 2, in this embodiment, the method to extract the transfer functions considers that the memory of previous processing is embedded in the state of the incoming wafer. In order to have a robust method of partitioning the coefficient vector of the measurement FP at the immediate process step, a set of incoming wafers may be generated by intentionally varying the process conditions at some earlier process step. For example, the measurement FP of a resist CD at a photoresist develop step is expected to correlate with the planarity of the wafer surface on which the resist pattern is being formed. Accordingly, process parameters of a previous planarization process step may be varied intentionally from the baseline process flow to generate incoming wafers, wherein each wafer has a different planarity FP obtained at the planarization step. The response of the coefficient vectors of the resist CD measurements to the variations in the planarity FP's of this specially prepared set of non-baseline incoming wafers is then analyzed to identify the sensitivity of the deviation of each coefficient of the resist CD FP from its baseline value. This information may be used to define a transformation matrix that may map the coefficient vector of planarity FP's of all incoming wafers onto a respective resist-CD response vector (referred to as the transferred vector) which is the part of the resist-CD coefficient vector that is expected to include all the correlation with the planarity FP of the wafer at the planarization step. This response vector captures the memory of the planarization process and may be subtracted from the resist-CD measurement FP to obtain the uncorrelated component (referred to as the immediate step vector) of the resist-CD coefficient vector that is expected to correlate more strongly with the processing conditions at the immediate process step.

[0066] The transformation matrix, in the example embodiment described above, is a mathematical implementation of a transfer function. It is understood, that other mathematical implementations are possible, as mentioned above.

[0067] The transfer functions for a particular baseline wafer fabrication process flow need not be generated each time a batch of wafers is processed by the wafer fabrication production line. The transfer functions may be generated once and stored

electronically to be available for future use. Periodically, the transfer functions may be updated as modifications are made to the baseline wafer fabrication process flow.

[0068] In the example embodiment illustrated by the flowchart in Figure 2, system 200 creates a process model for the process step from the response of the immediate step vectors of the measurement FP's of that step. The steps for creating this process model is outlined in blocks 250, 260, and 270 and described with reference to Figure 4.

[0069] In block 250, the system 200 obtains in-line fabrication measurement data from a set of wafers processed using several process parameter values at and around those prescribed in the baseline wafer fabrication process flow. Each process parameter is associated with different adjustable equipment settings at the process step for which the process model is to be created. For example, some process may allow the conditions (e.g., etch rate, etch time, gas concentration, etc.) to be adjusted based on controls available for one or more tools of the process. In that case, those process conditions are process parameters.

[0070] Figure 4A illustrates an example of raw data depicted graphically by a 4×4 matrix of wafer maps 400 of in-line measurement data. Each wafer map of the example matrix in Figure 4A corresponds to measurements of the same measurement type performed on one or more wafers processed using a specific process parameter vector comprising a pair of values for two process parameters, a first process parameter par1 and a second parameter par2. For example, par1 may be the etch rate, and par2 may be etch time. In general, the number of process parameters being varied may be other than two. Also, measurements of more than one measurement type may be performed. The raw data in Figure 4A is displayed such that the wafer maps along a row of the 4×4 matrix correspond to four parameter values for par1, while the parameter values for par2 remain unchanged; and the wafer maps along a column correspond to four parameter values for par2, while the parameter values for par1 remain unchanged.

[0071] Also in block 250, the system 200 generates FP models of the raw data obtained from a set of wafers processed using the different process parameter vectors, as described above with reference to Figure 4A. One FP model is generated

from raw data obtained from each process parameter vector. For example, the 16 histograms depicted in Figure 4B are the respective FP models of the raw data depicted by the 16 wafer maps depicted in Figure 4A. The model function is a 21 term series of Zernike functions, similar to that described with reference to Figure 1B. Each bar is a coefficient of a 21-component coefficient vector of a FP model for the measurement type corresponding to the respective process parameter vector (par1, par2).

[0072] Still referring to block 250, system 200 may utilize the available transfer functions for the baseline process flow to decompose the measurement FP coefficient vectors in Figure 4B to obtain the immediate step vector of each measurement FP by subtracting the transferred vector from the coefficient vector. As described above, in this embodiment, each coefficient of the coefficient vector is split or decomposed into two parts. A first part is equal to the respective coefficient of the transferred vector calculated using the transfer functions. The first part represents correlations with one or more FP's obtained at earlier process steps. The remaining second part is then equal to the respective coefficient of the immediate step vector that represents the part determined by the process conditions of the immediate process step. It is desirable to use the immediate step vectors to generate a process model in order to prevent the parameters of the process model of the immediate process step from being influenced by process parameters at one or more of the earlier process steps.

[0073] At block 260, the system 200 selects model functions to model the response of each coefficient of the immediate step vector of a fingerprint to changes in the process parameters (e.g., par1 and par2). A different model function may be used to model each of the coefficients of the immediate step vector, for example, the 21 coefficients of a 21-term series of Zernike polynomials denoted by a1, a2,... ai,... a20, a21 in Figure 4C. In the example illustrated in Figure 4, there are 16 instances for each coefficient, ai, corresponding to the 16 process vectors used at the process step in order to generate the 16 wafers and respective FP's.

[0074] The model parameters of the model functions selected at block 260 are adjusted in block 270 for the best fit to the 16 values of each coefficient, ai, to generate an optimized process model for the process step, the process model

comprising the 21 model functions denoted by f1, f2,... fi,... f20, f21 in Figure 4C. Each of the functions fi has been optimized in accordance with an optimization algorithm. The first two process models, f1 and f2, are depicted graphically in Figure 4C as three-dimensional (3D) surfaces plotted as a function of two process parameters, par1 and par2. The 16 points near each of the 3D surfaces are the 16 values a1, and a2 which were used to create the models f1 and f2, illustrate a good fit between the predictions of the process model and the coefficients of the immediate step vector of the FP model.

[0075] Figure 4D illustrates the wafer maps calculated from the FP models and the associated process model. A comparison of the wafer maps in Figure 4D with the wafer maps of the raw data in Figure 4A shows a good fit, thereby illustrating the predictive capability of the FP models along with the associated process model in reproducing the in-line fabrication metrology data, including its spatial information, over a process parameter space around a baseline processing condition.

[0076] The process model for process steps in a baseline wafer fabrication process flow may also be generated once and stored electronically to be available for future use, similar to the baseline transfer functions. Also similar to the transfer functions, periodically, the process model may be updated as modifications are made to the baseline process.

[0077] Fingerprints of the baseline in-line wafer fabrication metrology data may be generated more frequently for real-time yield analysis and advanced process control (APC), especially for process steps that strongly impact manufacturing yield. A reference set of FP's may be archived to compare with those obtained from the running production line to detect, analyze, and correct abnormalities.

[0078] At block 280 in the flowchart in Figure 2, the lowest level FP's (which are the measurement FP's) may be combined and calculations may be used to create higher level FP's and an associated process model capable of accurately predicting the relevant metrics of the process steps. In order to combine multiple FP's having different units, it may be necessary to normalize the values of the coefficients to obtain consistent units.

[0079] As described above, the FP models, transfer functions, and associated process model, generated using in-line measurements that include 2D spatial coordinates of the measurement locations can be used advantageously in a wafer fabrication manufacturing system. As mentioned earlier, and indicated in block 290, the system 200 may identify the dominant coefficients of the FP's and dominant parameters of the process model. This may help not only in simplifying the model by eliminating the less significant parameters of the model but also provide useful insight into the impact of the process parameters, equipment settings, and equipment selection on manufacturing yield. The models may be used in monitoring and ameliorating yield loss in conjunction with an APC tool, and even be used to improve the baseline wafer fabrication process flow to provide higher manufacturing yield, as described further below.

[0080] The flowchart in Figure 5 illustrates a portion of a flow that may be used to generate fingerprints of metrics for a process module or layer 500, for example, active layer, gate layer, contact layer, metal layer, and the like, each layer comprising one or more process steps. At each process step, the FP's, transfer functions, and process models, for the respective process step may be generated by the manufacturing system, such as the system 200, using, for example, the flow described with reference to the flowchart illustrated in Figure 2.

[0081] The FP's, transfer functions, and process model for the layer (e.g., layer 500) may be generated by combinations and calculations using the FP's, transfer functions, and process model for each process step. An example method of generating a layer FP is explained with reference to a flowchart in Figure 6.

[0082] In the example illustrated in Figure 5, the layer 500 comprises four representative process steps (A, B, C, D) such as resist coat, exposure, develop, resist strip, and the like. Although four process steps are shown for example purposes, the layer 500 may include any number of steps. The inputs provided to each process step are the incoming wafers along with the FP's and transfer functions generated at earlier process steps.

[0083] The process step (e.g., step A, B, C, or D) comprises processing equipment for wafer fabrication such as coater, scanner, plasma etcher, test equipment, and the

like, and associated chemicals, vacuum pumps, temperature controller, and the like, as known to a person skilled in the art. Along with the equipment, each process step includes process recipes comprising process parameter values, timing information, and instructions for processing the incoming wafers. The equipment has adjustable settings which may be used to control adjustable process parameters such as etch rate, gas flow, exposure level, spin speed, and the like. Each process parameter is represented in Figure 5 by a unique upper-case, italic subscript (J through U). For example, the adjustable process parameters for the process step A are AJ, AK, and AL, as seen in the first column in Figure 5.

[0084] One or more incoming wafers may be processed at a process step by executing one or more process recipe selected to obtain a desired outcome, for example, deposit a film of a desired material and thickness. The processing may be monitored using various sensors, and the processing equipment may be controlled by an APC system to ensure that the process parameters achieve outcomes as intended by the process recipe. By default, the wafers are processed in accordance with a baseline process recipe of the baseline wafer fabrication process flow.

[0085] As described above, in-line measurements of wafer characteristics are collected as the first step in the FP model generation flowchart in Figure 2. Measurements of multiple types may be done (e.g., deposited film thickness, resist CD of a first line, resist CD of a second line, step-height, leakage current, and the like), each measurement type having a unique letter as subscript. There are eight measurement types shown in Figure 5 denoted by eight subscripts (a through h). The in-line wafer fabrication metrology data may be gathered from multiple wafers, but the set of locations on a wafer may be the same for all wafers measured at a given process step (e.g., step A) and for a fixed measurement type (e.g., type a). The spatial information is retained by associating each data point with the 2D spatial coordinates of the location on the wafer from where the data was acquired.

[0086] In Figure 5, each data point of the same measurement type is identified by a unique italicized numeral as superscript (1, 2, 3, 4, etc.). Accordingly, the set of wafer measurements of type a (including the spatial information) at process step A is denoted by {Aa1, Aa2, Aa3, Aa4...}. In the example in Figure 5, two types of

measurements are performed at each of the four process steps, a total of eight types in the process module 500.

[0087] The lowest level FP models may be generated from the in-line wafer fabrication metrology data at each step, for example, at step A there may be two measurement FP's: one FP for the dataset {Aa1, Aa2, Aa3, Aa4...} and another FP for the dataset {Ab1, Ab2, Ab3, Ab4...}. Fingerprints for the process step created using combinations and calculations of the measurement FP's are denoted in Figure 5 by the process step name with the subscript FP and a numeric superscript to identify each process step fingerprint. For example, in Figure 5, the two process step FP's at step A are shown as AFP1 and AFP2. Various combinations of the two measurement sets Aan and Abn can be used to arrive at the two process step fingerprints. For instance, in one case, measurement set Aan is used to create process step fingerprint AFP1, and measurement set Abn is used to create process step fingerprint AFP2. In another case, measurement sets Aan and Abn are used together to create process step fingerprint AFP1, and either measurement set Abn or Abn alone is used to create process step fingerprint AFP2. Multiple other combinations are also possible, with each process step fingerprint being created from one or more sets of wafer measurements, using various weighting, scaling, averaging, fitting and/or other techniques. Although two process step fingerprints are shown for each process step for example purposes, each process step may include one or more process step fingerprints.

[0088] Transfer functions for each process step may be generated from the correlations between the FP models generated at earlier process steps and the measurement FP's of the immediate process step. One example method of identifying the correlations, explained in the description of the flowchart in Figure 2, comprises generating a set of non-baseline wafers by intentionally varying the process parameters at an earlier process step (e.g., step B in Figure 5) and then using the wafers as incoming wafers processed at the immediate process step (e.g., step C) using the baseline process recipe. The response of the measurement FP's at the immediate step C to the intentional variations in the FP's at the previous step B provides the information to generate a transformation matrix as the transfer function that predicts changes in the measurable outcomes of process C from the wafer

characteristics observed at process step B. As mentioned above, it may be possible to define other methods to generate transfer functions other than transformation matrices to model the influence of wafer characteristics at one process step (e.g., step B) on the outcomes of processing at a subsequent process step (e.g., step C).

[0089] Once all the transfer functions for a process step (e.g., step A to be specific) are defined, each measurement FP of step A, represented by a respective coefficient vector, may be decomposed into a transferred vector that correlates with previous processing and an immediate step vector that is decoupled from the process parameters of previous process steps. This decoupling provides the advantage of creating an accurate process model for step A from a set of in-line wafer metrology data obtained from a set of wafers fabricated by varying only the process parameter vector (AJ, AK, AL) of step A, using the method described above with reference to Figures 2 and 4.

[0090] It is understood that the description and explanation of methods by which fingerprints, transfer functions, and process models of a process step or a layer comprising a collection of process steps may be generated are provided herein as examples and should not be considered as limiting. As mentioned above, methods other than the described methods are also possible and these alternative methods may be derived from the descriptions and explanations provided in this disclosure.

[0091] The process models for the lower level measurement FP's may be extended to create a process model for the higher level FP's derived from the measurement FP's. The combinations and calculations used to generate the two process step FP's AFP1 and AFP2 may be utilized to create a process model for the process step A by respective combinations and calculations of process models for the measurement FP's.

[0092] Figures 6A-6C illustrates an example of the method by which a hierarchy of FP's may be generated by combinations and calculations of lower level FP's. In particular, a layer-level FP for EPE (referred to as EPEA) is generated in Figure 6 starting from measurement FP's (the lowest level) obtained from in-line measurements using a flowchart illustrated in Figure 6A. An example equation that may be used to compute EPEA is displayed in Figure 6B. Figure 6C illustrates a

perspective view of a fabricated structure to explain that the in-line wafer fabrication metrology data used to obtain the measurement FP's may be collected at different process steps. In this example, the process steps belong to a process module, referred to as the metal-1 layer. The raw in-line data are collected from measurements involving two patterned films formed in the metal-1 layer, a first film A and a second film B, illustrated in Figure 6C.

[0093] Five fingerprints, collectively shown as FP's 670, form the set of measurement FP's {612, 622, 623, 632, 633} from which higher level FP's are obtained in the flowchart illustrated in Figure 6A. Higher level FP's, 611, 621, 631, and 641, are generated in the flow in Figure 6A from the measurement FP's 670 using various comparisons, calculations or other processes, collectively indicated as the comparisons, calculations, etc. 660. These fingerprints may be further compared and processed to arrive at aggregate, representative or resulting fingerprints for overlay (OL)AB 610, pitch walk (PwalkA) 620, variable A (VarA) 630 (e.g., a trench critical dimension (CD)), and variable B (VarB) 640 (e.g. CD of a block). The subscripts A and B refer to metrics pertaining to the films A and B, respectively, and subscript AB is used for metrics which involve both the films A and B.

[0094] As next illustrated in the equation displayed in Figure 6B, the FP's 610, 620, 630, and 640 are used to calculate a fingerprint EPEA, which is the layer-level fingerprint for the edge placement error for the patterned film A. Methods, similar to the method explained herein may be applied to generate other fingerprints relevant to the wafer fabrication manufacturing system and the manufacturing yield of the baseline process flow.

[0095] The elements of the set of measurement FP's in the example flowchart in Figure 6A are Overlay 612, Line #4 CD 622, Line #5 CD 623, Trench #4 CD 632 and Block 1T CD 642. The raw in-line wafer fabrication metrology data for these measurement FP's involve two patterned films, a first patterned film A (formed using a self-aligned quadruple patterning (SAQP) technique) and a second patterned film B, as illustrated in Figure 6C. Measurement FP Overlay 612 uses measurements of overlay error between these two patterns. Fingerprints Line #4 CD 622 and Line #5 CD 623 are extracted from line and space measurements gathered at one or more of the SAQP process steps performed to form the patterned film A and used

subsequently to calculate a multiple-patterning metric called pitch-walk. The FP Trench #4 CD 632 may be generated from measurements of the space between a pair of adjacent lines of the patterned film A in Figure 6C created by a processing technique comprising formation of a pair of self-aligned spacers on the opposing sides of a disposable mandrel. Fingerprint Block 1T CD 642 uses linewidth measurements of a geometric feature involving critical dimension in the pattern of the patterned film B in Figure 6C. It is apparent from the description of the measurements provided herein that the resultant layer FP EPEA incorporates in-line wafer fabrication metrology data gathered at different process steps.

[0096] Still referring to Figure 6A, the higher level FP's 611, 621, 631, and 641, generated using various comparisons, calculations, and combinations 660, represent several metrics relevant for calculating the edge placement error of a feature in the pattern of the patterned film A. A magnitude of the y-overlay error derived from Overlay 612 is represented by FP 611; a magnitude of pitch-walk in film A derived from Line #4 CD 622 and Line #5 CD 623 is represented by FP 621; Trench #4 CD 632 determines a magnitude of a geometric variable/CD 631 in Film A; and Block 1T CD 642 determines a magnitude of a geometric variable/CD 641 in Film B. The comparisons, calculations and combinations may be of various types, for example, simple algebraic operations, analytic linear and non-linear functions, vector functions, geometric transformations, statistical analysis, computer algorithms of numerical methods, or the like, or combinations thereof.

[0097] As mentioned above, the higher level FP's may be further processed to arrive at the fingerprints (OL)AB 610, PwalkA 620, VarA 630, and VarB 640, which are used in the exemplary equation 680 displayed in Figure 6B. This exemplary equation defines a metal-1 layer-level FP, EPEA, which may be used to compute the edge placement error for the layer. In this equation, (MP)A refers to the geometric line-space ratio of minimum pitch lines, PregA refers to pattern registration error (a patterning error originating from the photomask, hence the same error is repeated on every exposure field), and LspecA represents a geometric line specification from the pattern design. In the equation 680, VarA, VarB, PregA, (OL)AB, and PwalkA are fingerprints, and (MP)A and LspecA are constants. The items PregA, (MP)A, and LspecA are additional fingerprints /constants not illustrated in Figure 6A but are used

in equation 680 as an illustration. The equation may include various constants obtained from independent sources such as specification documents for the photomask, manufacturer's specifications for processing equipment, and the like.

[0098] Layer-level FP's, such as the layer-level FP EPEA, may be used to perform a pareto analysis to identify the dominant factors affecting the metrics of the layer, and thereby the manufacturing yield. For example, calculations using the equation in Figure 6B can rank order the contributions of overlay error, pitch-walk in the pattern of film A, variability in trench width of trenches in film A, and linewidth variations of lines in film B to the EPE of the layer. In one example, such a pareto analysis reveals that the most dominant factor is the overlay error contributing about 55 % of the total edge placement error, and that the impact of trench width variation is negligible with a contribution of only about 1 %. In this example, the contributions to the EPE are aggregates obtained by combining all spatial locations on the wafer. More targeted analysis may be performed which may further analyze the yield loss at particularly vulnerable regions on the wafer, for example, the region near the edge of the wafer. Such analyses can be used to improve the baseline process flow and manufacturing yield.

[0099] A more general flowchart illustrated in Figure 7 describes an embodiment of a flow whereby a system 700 may extend the methods and techniques described above to create transfer functions and process models for a process step to create transfer functions and process models to predict fingerprints of metrics and hence, wafer characteristics at any step in the baseline wafer fabrication process flow.

[00100] At block 710 of the flowchart in Figure 7, in-line measurements with associated spatial information is obtained from wafers processed in accordance with the baseline process flow. This in-line wafer fabrication metrology data may be used to generate measurement FP's and higher level FP's characterizing the entire baseline process flow, as indicated in block 720. Then, at block 730, non-baseline wafers may be generated by varying the process parameters at the process steps of the baseline process flow. Since advanced process flows are complex, involving hundreds of process steps, it may be advantageous to first identify dominant process steps that affect manufacturing yield using, for example, a pareto analysis similar to the one described above utilizing the equation for the layer-level fingerprint EPE,

displayed in Figure 6B. At block 740, the in-line measurements and respective fingerprints are obtained using the wafer metrology data and associated process parameter values of the non-baseline wafers generated at block 730.

[00101] Subsequent blocks in Figure 7 illustrate how the information captured from the in-line measurements with associated spatial coordinates and process parameter values may be utilized to create a predictive model for the baseline process flow.

[00102] At block 750, transfer functions are created to model correlations between variations in wafer characteristics at one process step with wafer characteristics at a subsequent process step. The variations at the earlier process step may be caused either by natural deviations in processing conditions or generated intentionally by varying adjustable process parameters. The responses of all the coefficients or parameters of a fingerprint to the process parameters intentionally varied at a specific process step are obtained at block 760.

[00103] At block 770, the component of the fingerprint responses that correlate with processing at previous process steps is calculated from the transfer functions. Then the component that is uncorrelated to the earlier process steps may be partitioned out. This component is fit to a mathematical model to obtain a process model of the immediate process step.

[00104] Process models for all the process steps which may have been selected at block 730 as a dominant process step may be generated using the method described above, as indicated in block 780. At block 780, the wafer characteristics with associated spatial information at any step of the baseline process flow may be predicted using the baseline fingerprints, transfer functions, and process models.

[00105] The fingerprints, transfer functions, and process models collectively provide a mathematical model for a wafer fabrication process flow that may be used by a wafer manufacturing system. Once such a model is created, it can be used by a manufacturing system to predict, optimize, adjust and/or control one or more of the process steps in order to achieve desired improvements in the manufacturing yield in production of wafers. In other words, using the model, process conditions may be

modified / altered and thus a plurality of wafers comprising semiconductor dies can be manufactured at a higher yield resulting in a decrease in manufacturing costs.

[00106] For example, dominant process steps identified by analyzing the baseline fingerprints may be monitored more frequently. The fingerprints generated from in-line metrology data collected for monitoring the production line may not only detect wafers that fail specification (referred to as non-conformity) but also identify the spatial coordinates of regions of high non-conformity or high density of non-conformities. Such information is advantageous in detection and determination of systemic non-conformities. The process models may be used to identify one more pieces of equipment which could be possible sources of manufacturing yield loss and provide the information for the system to adopt a single-tool or a multi-tool process control strategy. Moreover, when used in conjunction with an APC tool, the model may assist the manufacturing system to suggest or recommend adjustments to the particular process parameters for amelioration of non-conformities to recover the yield loss. In some instances, the system may directly adjust the particular process parameters.

[00107] Additionally, the process model and transfer function may be used to improve the baseline process flow. For example, the system may use the process model to optimize process parameters so that the optimized fingerprint improves a target metric, such as EPE. The optimized process parameters may be fed into the process as the new plan-of-record (POR) thereby improving the manufacturing yield of the baseline process flow.

[00108] This may be described in this manner: The system obtains a target range of values of the associated predicable characteristics of a target semiconductor wafer. This target range is the range of acceptable or desirable values for an acceptable or desirable semiconductor wafer produced by the semiconductor wafer fabrication process. For example, a customer may specify the range of acceptable values for EPE.

[00109] Using the process model, the system optimizes one or more of the process parameters of semiconductor wafer fingerprints so that the values of associated predicable characteristics of the semiconductor wafers produced by the

semiconductor wafer fabrication process fall within the obtained target range. That is, using the process model, the system calculates a value of one or more of the process parameters that effectively produce the values of the associated predicable characteristics that would fall within the obtained target range. Of course, in some implementations, range may be a plus/minus range about a target value.

[00110] Furthermore, because this process model preserves the spatial characteristics the process parameters which affect the EPE at specific regions of high non-conformities may be identified and adjusted for improved manufacturing yield.

[00111] The methods illustrated in Figures 2 and 7 as well as the associated Figures 1, 3-6 may be implemented in or using a non-transitory computer-readable storage medium comprising instructions that when executed cause a processor of a computing device to perform operations in coordination with a semiconductor wafer fabrication process. In addition, some of the instructions for performing the steps of Figures 2 and 7 may be stored in separate locations in different non-transitory computer-readable storage medium and may be configured to be performed in different processors of different computing devices. Examples of non-transitory computer-readable storage medium include various types of memories including non-volatile solid state memories, and other storage mediums. For example, non-transitory computer-readable storage medium may include, but are not limited to, magnetic storage devices (e.g., hard disk, floppy disk, and magnetic strips), optical disks (e.g., compact disk (CD) and digital versatile disk (DVD)), smart cards, flash memory devices (e.g., thumb drive, stick, key drive, and Secure Digital (SD) cards), and volatile and non-volatile memory (e.g., random access memory (RAM), read-only memory (ROM)).

[00112] For example, the steps 220 to 290 of Figure 2 may be instructions that are configured to be executed in one or more processors, which result in the developing of a process model. Similarly, the steps 720 to 780 of Figure 7 may be instructions that may be configured to be executed in one or more processors, which result in the developing of a process model.

[00113] The techniques described with relation to Figures 1-7 describe methods for generating fingerprints and creating a process mode using fingerprints. In one application of a fingerprint based model, a method to detect any anomalies of a process or process tools may be provided. In another embodiment of an application of the fingerprint based model, a method to detect defects is provided.

[00114] Sensitivity calculations of a process model through the rate of change of a model fingerprint with respect to process variables are provided. A table of fingerprint sensitivities is generated, where process variables are associated with a set of fingerprint sensitivity. The fingerprint of incoming substrates is monitored through a production process by applying the same fingerprint method that is used in the process model. Calculations are made of the difference between the incoming substrate fingerprint and the predicted fingerprint which is calculated using the process model. This difference fingerprint is compared against the table of fingerprint sensitivities to find the process variable most likely to be responsible for the difference. A chart that ranks this likelihood may then be created and reported to the user. Spatial relationships between process variables and actual measurements on the substrate may be obtained. Direct correlation through fingerprint sensitivity improves the ability to pinpoint faulty process tools. In another alternative, the fingerprint process may be utilized to detect defects which have formed on the substrate. For example, particulates that may form on a substrate at a particular process step may be detected through use of the fingerprint comparison process described herein.

[00115] Faulty process tools (or parts of the process tool) may have significant impact on the fingerprint of the processed substrate. Similarly defects may have significant impact on the fingerprint of the processed substrate. The disclosed methods present the detail of using fingerprint modeling to detect process variable related drifts to identify faulty process tools and/or parts early and/or to detect the formation of defects at a process step. The technique disclosed does not require sensor input to detect faulty tools and/or defects. Thus, an alternative method to identify root causes of a substrate processing process problem or faulty tools and/or parts by isolating process variables with contributing fingerprint components and detection based on the process variable sensitivity is provided. Similarly, the

disclosed methods present the detail of using fingerprint modeling to detect the formation of defects at a process step. The technique disclosed does not require sensor input to the defects. Thus, an alternative method to identify a substrate processing problems forming defects by use of fingerprint techniques is provided.

[00116] In one embodiment for process fault detection, after a process model is created (for example as described above), the method and systems involve calculating the sensitivity of the process model through the rate of change of fingerprint with respect to each process variable (or "knob"). A table of fingerprint sensitivities is generated through this method, where each process variable is associated with a set of fingerprint sensitivity. This table may be stored for use in a monitoring step as described below.

[00117] In one embodiment, the system monitors the fingerprint of incoming substrates (for example an incoming semiconductor wafer) through the production line by applying the same fingerprint method that is used in the process model. Then, the system calculates the difference between the incoming wafer fingerprint and the predicted fingerprint which is calculated using the process model. This difference fingerprint is compared against the table of fingerprint sensitivities to find the process variable most likely to be responsible for the difference. A chart that ranks this likelihood may then be created and reported to the user.

[00118] The method to generate such chart that reports process variable related fault correlation is unique in that it does not rely on sensors other than the measured metrology. Traditional methods using sensors depend on other types of measurements that only indirectly impact the substrate. The fingerprint based method is capable of detecting spatial relationships between process variables and actual measurements on the substrate. The direct correlation through fingerprint sensitivity improves the ability to pinpoint faulty process parts and early detection of poor wafer performance.

[00119] Faulty process tools (or parts of the process tool) may have significant impact on the fingerprint of the processed wafer. The disclosed methods presents the detail of using fingerprint modeling to detect process variable related drifts to identify faulty process tools and/or parts early. The technique disclosed does not

require sensor input to detect faulty tools and/or parts. Thus, an alternative method to identify root causes of a substrate processing process problem or faulty tools and/or parts by isolating process variables with contributing fingerprint components and detection based on the process variable sensitivity is provided.

[00120] Figure 8 illustrates an exemplary work flow diagram for implementing a fingerprint based fault detection technique for use with semiconductor wafers. As shown in Figure 8, design of experiment is first performed in step 800 for one or more process steps of a semiconductor process flow. The experimental design may account for a wide variety of process conditions and variables for which potential changes or fluctuations may be expected to occur in a typical process environment. The experimental process may vary those process conditions and variables singularly and/or in various combinations on a number of different experiment wafers. For each wafer in the experiment, wafer data may then be collected as shown in step 805. As shown in step 810 a fingerprint may be created. Using the experimental data, a process model is created in step 815. The process model may provide a fingerprint component as a function of all process conditions.

[00121] When the process model is created in step 815 of Figure 8, that process model may be applied to wafers utilized in a production manufacturing process. Thus, for each wafer of the production manufacturing process at a particular point of a manufacturing process flow, wafer data may be collected as shown in step 820. Then as shown in step 825 the fingerprint may be created. Utilizing the process model created in step 815, a difference between the fingerprint of step 825 and the calculated modeled fingerprint step 830 may be created at step 835. The techniques described above with regard to Figures 1-7 may be utilized to create the calculated difference of step 835.

[00122] Then, the calculated difference of step 835 may be utilized in conjunction with the process model of step 815 so that in step 840 a comparison of the calculated difference is made against the process model sensitivity is made. The comparison of step 840 may then be used in step 845 to detect the faulty process variable ("knob") that caused the differences detected on the wafer fingerprint as compared to the expected modeled fingerprint. In this manner, the fingerprint

process may be utilized to detect faults in the process flow that caused changes to the wafer fingerprint.

[00123] Figures 9-14 provide an exemplary application of the techniques described herein. More specifically, these figures illustrate an example process step in which a film is formed on a semiconductor wafer. The example illustrates the usage of the fingerprint model to detect a faulty process variable of the film formation process. Semiconductor processing techniques include a wide range of process variables for each particular process step (steps such as but not limited to surface preparation, ion implantation, thermal steps (e.g., rapid thermal oxidation (RTO), rapid thermal anneal (RTA), laser anneal, etc.), photolithography steps (e.g., resist coat, exposure, develop, resist strip, etc.), electroplating, plasma deposition, plasma etch, wet etch, chemical mechanical polish (CMP), and the like). The particular process variables for any of the these process steps may be wide ranging, including but not limited to temperatures, pressures, gasses, gas flow rates, power settings, voltage settings, current settings, spin speeds, dispense volumes, liquids, liquid flow rates, liquid density, time, etc. Moreover, any particular process step may be comprised of a series of sub-steps each having a set of variables for each sub-step (for example a plasma etch process or a plasma deposition process may be comprised of two, three, four or even more steps).

[00124] Figure 9 illustrates an exemplary table illustrating a variety of process variables (in this case 19 process model terms 900 indicated as Par 1-Par 19) for a film formation process. As shown in Figure 9, the terms are listed by sensitivity rank (a smaller rank being more sensitive). In the example shown, Par 4 has the smallest rank and is thus the most sensitive. The corresponding fingerprint terms 905 are also shown. Figure 10 illustrates the film thickness raw data spatially collected across a grid of a monitor wafer. Figure 10 also illustrates the corresponding coefficient strength 1020 and coefficients 1030 as provided by the fingerprint model 1040.

[00125] With reference to the work flow diagram of Figure 8, the coefficient strength 1020 and coefficients 1030 of Figure 10 provide the fingerprint of step 825 of Figure 8. Figures 11A and 11B illustrate the work flow steps 825, 830 and 835 of Figure 8 with regard to the film thickness example. More particular, Figure 11A illustrates the steps as applied a presumed “good” wafer, in this example a wafer

processed without a process fault. Figure 11B illustrates the steps as applied for a "bad" wafer in which a process fault occurred during processing. As shown in Figure 11A the coefficients and coefficient strengths of a good wafer create a fingerprint 1110 (such as step 825 of Figure 8). Predicted coefficients and coefficients strength a calculated using the process model to create a modeled fingerprint 1120 (such as step 830 of Figure 8). Then a difference fingerprint 1130 is obtained by calculating the difference between the fingerprint 1110 and modeled fingerprint 1120. Figure 11B illustrates the work flow steps, as applied in this example, to a wafer that was subjected to a faulty production process. As shown in Figure 11B the coefficients and coefficient strengths of a bad wafer create a fingerprint 1140 (such as step 825 of Figure 8). Predicted coefficients and coefficients strength a calculated using the process model to create a modeled fingerprint 1150 (such as step 830 of Figure 8). Then a difference fingerprint 1160 is obtained by calculating the difference between the fingerprint 1140 and modeled fingerprint 1150.

[00126] The difference fingerprints (for example difference fingerprint 1130 of Figure 11A and difference fingerprint 1160 of Figure 11B) may then be compared against the process model sensitivity to help determine if a particular process variable is faulty. Figures 12A and 12B illustrate exemplary results of such a comparison. For example, using the difference fingerprint 1130 may show that any differences from the predicted fingerprint are not driven by any one (or set) of faulty process variables. As shown in Figure 12A, the 19 process variables ("process model terms") indicate that no one process model exhibits a high probability of being faulty. More particularly, Figure 12A illustrates a chart 1210 plotting the process variable (process model term 1202) against the probability of fault 1204 for a particular process variable. In this example, as the wafer analyzed was a "good" wafer, one that did not exhibit a particular poor spatial film thickness profile indicative of a fault, no particular process variables exhibit a distinctive high level of probability of fault. Based on the analysis, the differences between the actual wafer and the modeled results do not show any particular faulty process variable. Figure 12B, however, the probabilities for the "bad" wafer, demonstrating a detected fault. More particularly, Figure 12B illustrates a chart 12200 plotting the process variable (process model term 1202) against the probability of fault 1204 for a particular process variable. In this example, a fault with one of the process variables has been

detected. As shown, a high fault likelihood 1230 of over 90% is shown from process model term 10. Based on the analysis, the differences between the actual wafer (the bad wafer in this case) and the modeled results indicate a fault with regard to process variable 10. In this manner, faults in the processing of the wafer may be detected and identified utilizing the fingerprint techniques. Predetermined fault probability levels may be established for each process variable to identify when a process variable is to be identified as faulty.

[00127] As mentioned above, the fingerprint analysis techniques described herein may also be utilized to identify localized defects on a wafer, such as for example, caused particles, pattern collapse, voids, hotspots, etc. More particularly, the process modeling techniques described herein may be combined with defect detection techniques. Though defect detection may be identified by looking for spatially localized large spikes in data obtained from a wafer, such techniques may result in false defect detection. To reduce false defect detections, potential process variable fluctuations may also be combined with the analysis. Thus, the process model that is created through the design of experiment process is utilized in the defect analysis process. By accounting for variations in the process variables, a more robust defect detection process may be achieved that reduces the occurrences of false positives.

[00128] Figure 13 illustrates an exemplary work flow diagram for implementing a fingerprint based defect detection technique for use with semiconductor wafers similar to the fault detection technique of Figure 8. As shown in Figure 13, similar steps 800, 805, 810, and 815 are used as in Figure 8 to create a process model. Likewise, steps 820, 830 and 835 may be utilized as shown in Figure 13 similar to those same step numbers of Figure 8. It is noted that for the production wafer a fingerprint creation step is not needed as for defects are associated with a local high frequency spike and fingerprints typically capture long range spatial variations. Thus, the calculated difference of step 835 may be obtained from the wafer data collected at step 820 and the modeled fingerprint calculated at step 830. With the calculated difference obtained at step 835, defects may then be detected at step 1310 through analysis of the calculated difference and consideration of potential process variable change impacts provided from the process model. In this manner, spatially local

spikes in the data may more confidently be identified as defects because the analysis accounts for impact of potential process variable changes In this manner, fingerprint based defect detection may be utilized to provide a more accurate assessment of the presence defects.

[00129] Figures 14-16 illustrate exemplary methods for use of the processing techniques described herein. It will be recognized that the embodiments of Figures 14-16 are merely exemplary and additional methods may utilize the techniques described herein. Further, additional processing steps may be added to the methods shown in the Figures 14-16 as the steps described are not intended to be exclusive. Moreover, the order of the steps is not limited to the order shown in Figures 14-16 as different orders may occur and/or various steps may be performed in combination or at the same time.

[00130] Figure 14 illustrates a method of characterizing a fabrication process for manufacturing a semiconductor wafer, the fabrication process comprising at least one process step, the at least one process step being associated with a plurality of process variables. As shown in the figure, step 1405 comprises performing a design of experiment process for the at least one process step, wherein the plurality of process variables are changed for a plurality of design of experiment semiconductor wafers. Step 1410 includes obtaining design of experiment wafer measurements of a first characteristic from the plurality of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the measurement is obtained. Step 1415 includes creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints. Step 1420 includes creating a process model of the at least one process step utilizing the plurality of design of experiment process step fingerprints. Step 1425 includes performing the at least one process step on a production semiconductor wafer. Step 1430 includes obtaining production wafer measurements of the first characteristic of the production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the production semiconductor wafer from which

the measurement is obtained. Step 1435 includes creating a production semiconductor wafer process step fingerprint from the obtained production semiconductor wafer measurements. Step 1440 includes detecting a faulty process variable of the at least one process step utilizing the production semiconductor wafer process step fingerprint and the process model.

[00131] Figure 15 illustrates a method of characterizing a fabrication process for manufacturing a semiconductor wafer, the fabrication process comprising a plurality of process steps, at least a first one of the plurality of process steps being associated with a plurality of process variables. The method includes performing a design of experiment process, the design of experiment process comprising steps 1505 through 1520. Step 1505 includes for a series of design of experiment semiconductor wafers, performing the first one of the plurality of process steps on the series of design of experiment semiconductor wafers, wherein at least one or more of the values of the plurality of process variables are changed for each of the series of design of experiment semiconductor wafers. Step 1510 includes obtaining design of experiment wafer measurements of a first characteristic from the series of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the design of experiment wafer measurement is obtained. Step 1515 includes creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints. Step 1520 includes creating a process model of the first one of the plurality of process steps utilizing the plurality of design of experiment process step fingerprints. Then the method comprises step 1525 of performing the first one of the plurality of process steps on at least one production semiconductor wafer. Step 1530 comprises obtaining production wafer measurements of the first characteristic of the production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the production semiconductor wafer from which the measurement is obtained. Step 1535 comprises creating a production wafer process step fingerprint from the obtained production wafer measurements. Step

1540 includes detecting a faulty process variable utilizing the production wafer process step fingerprint and the process model.

[00132] Figure 16 illustrates a method comprising of characterizing a fabrication process for manufacturing a semiconductor wafers, the fabrication process comprising a plurality of process steps, at least a first one of the plurality of process steps being associated with a plurality of process variables. The method includes performing a design of experiment process, the design of experiment process comprising steps 1605 through 1620. Step 1605 includes, for a series of design of experiment semiconductor wafers, performing the first one of the plurality of process steps on the series of design of experiment semiconductor wafers, wherein at least one or more of the values of the plurality of process variables are changed for each of the series of design of experiment semiconductor wafers. Step 1610 includes obtaining design of experiment wafer measurements of a first characteristic from the series of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the design of experiment measurement is obtained. Step 1615 includes creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints. Step 1620 includes creating a process model of the first one of the plurality of process steps utilizing the plurality of design of experiment process step fingerprints. Step 1625 includes performing the first one of the plurality of process steps on at least one production semiconductor wafer. Step 1630 includes obtaining production wafer measurements of the first characteristic of the at least one production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the at least one production semiconductor wafer from which the measurement is obtained. Step 1635 includes calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of first one of the plurality of process steps. Step 1640 includes detecting a defect on the at least one production semiconductor wafer utilizing the calculated modeled fingerprint for the production semiconductor wafer and the process model, wherein the process model is utilized

to account for process variable variations so as to improve the defect detection accuracy.

[00133] The substrates utilized with the techniques disclosed herein may be any substrates for which the etching and patterning of material is desirable. For example, in one embodiment, the substrate may be a semiconductor substrate having one or more semiconductor processing layers (all of which together may comprise the substrate) formed thereon. In one embodiment, the substrate may be a substrate that has been subject to multiple semiconductor processing steps which yield a wide variety of structures and layers, all of which are known in the substrate processing art. In one embodiment, the substrate may be a semiconductor wafer including the various structures and layers formed. In one example, microelectronic devices are formed on the substrates.

[00134] Further modifications and alternative embodiments of the inventions will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the manner of carrying out the inventions. It is to be understood that the forms and method of the inventions herein shown and described are to be taken as presently preferred embodiments. Equivalent techniques may be substituted for those illustrated and described herein and certain features of the inventions may be utilized independently of the use of other features, all as would be apparent to one skilled in the art after having the benefit of this description of the inventions.

What is claimed is:

1. A method of characterizing a fabrication process for manufacturing a semiconductor wafer, the fabrication process comprising at least one process step, the at least one process step being associated with a plurality of process variables, the method comprising:

performing a design of experiment process for the at least one process step, wherein the plurality of process variables are changed for a plurality of design of experiment semiconductor wafers;

obtaining design of experiment wafer measurements of a first characteristic from the plurality of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the measurement is obtained;

creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints;

creating a process model of the at least one process step utilizing the plurality of design of experiment process step fingerprints;

performing the at least one process step on a production semiconductor wafer;

obtaining production wafer measurements of the first characteristic of the production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the production semiconductor wafer from which the measurement is obtained;

creating a production semiconductor wafer process step fingerprint from the obtained production semiconductor wafer measurements; and

detecting a faulty process variable of the at least one process step utilizing the production semiconductor wafer process step fingerprint and the process model.

2. The method of claim 1, further comprising calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of the at least one process step.

3. The method of claim 2, further comprising:

calculating a difference between the modeled fingerprint and the production semiconductor wafer process step fingerprint; and

utilizing the calculated difference when detecting the faulty process variable of the at least one process step.

4. The method of claim 3, wherein the faulty process variable is detected by comparing the calculated difference against a process model sensitivity to help determine if a particular process variable is faulty.

5. The method of claim 4, wherein the particular process variable is identified utilizing a probability determination.

6. The method of claim 5, wherein the particular process variable is identified by analyzing a plurality of process model terms obtained by comparing the calculated difference against the process model sensitivity, to identify a process variable exceeding a predetermined fault probability level.

7. A method of characterizing a fabrication process for manufacturing a semiconductor wafer, the fabrication process comprising a plurality of process steps, at least a first one of the plurality of process steps being associated with a plurality of process variables, the method comprising:

performing a design of experiment process, the design of experiment process comprising:

for a series of design of experiment semiconductor wafers, performing the first one of the plurality of process steps on the series of design of experiment semiconductor wafers, wherein at least one or more of values of the plurality of process variables are changed for each of the series of design of experiment semiconductor wafers;

obtaining design of experiment wafer measurements of a first characteristic from the series of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the design of experiment wafer measurement is obtained;

creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints; and

creating a process model of the first one of the plurality of process steps utilizing the plurality of design of experiment process step fingerprints;

performing the first one of the plurality of process steps on at least one production semiconductor wafer;

obtaining production wafer measurements of the first characteristic of the production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the production semiconductor wafer from which the measurement is obtained;

creating a production wafer process step fingerprint from the obtained production wafer measurements; and

detecting a faulty process variable utilizing the production wafer process step fingerprint and the process model.

8. The method of claim 7, further comprising calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of the first one of the plurality of process steps.

9. The method of claim 8, further comprising:

calculating a difference between the modeled fingerprint and the production wafer process step fingerprint.

10. The method of claim 8, further comprising:

calculating a difference between the modeled fingerprint and the production wafer process step fingerprint; and

utilizing the calculated difference when detecting the faulty process variable of the first one of the plurality of process steps.

11. The method of claim 10, wherein the faulty process variable is detected by comparing the calculated difference against variable sensitivity levels of the process model to help determine that a particular process variable is the faulty process variable.

12. The method of claim 11, wherein the faulty process variable is identified utilizing a probability determination.

13. The method of claim 12, wherein the faulty process variable is identified by analyzing a plurality of process model terms obtained by comparing the calculated difference against the variable sensitivity levels, to identify a process variable exceeding a predetermined fault probability level.

14. The method of claim 8, wherein the faulty process variable is identified utilizing a probability determination.

15. The method of claim 14, wherein the faulty process variable is identified by analyzing a plurality of process model terms obtained by comparing the calculated difference against the variable sensitivity levels, to identify a process variable exceeding a predetermined fault probability level.

16. A method of characterizing a fabrication process for manufacturing a semiconductor wafers, the fabrication process comprising a plurality of process steps, at least a first one of the plurality of process steps being associated with a plurality of process variables, the method comprising:

performing a design of experiment process, the design of experiment process comprising:

for a series of design of experiment semiconductor wafers, performing the first one of the plurality of process steps on the series of

design of experiment semiconductor wafers, wherein at least one or more of values of the plurality of process variables are changed for each of the series of design of experiment semiconductor wafers;

obtaining design of experiment wafer measurements of a first characteristic from the series of design of experiment semiconductor wafers wherein each of the design of experiment wafer measurements is associated with a spatial location on the design of experiment semiconductor wafer from which the design of experiment measurement is obtained;

creating a design of experiment process step fingerprint from the obtained design of experiment wafer measurements for each design of experiment semiconductor wafer to provide a plurality of design of experiment process step fingerprints; and

creating a process model of the first one of the plurality of process steps utilizing the from the plurality of design of experiment process step fingerprints;

performing the first one of the plurality of process steps on at least one production semiconductor wafer;

obtaining production wafer measurements of the first characteristic of the at least one production semiconductor wafer wherein each of the production wafer measurements is associated with a spatial location on the at least one production semiconductor wafer from which the measurement is obtained;

calculating a modeled fingerprint for the production semiconductor wafer utilizing the process model of first one of the plurality of process steps; and

detecting a defect on the at least one production semiconductor wafer utilizing the calculated modeled fingerprint for the at least one production semiconductor wafer and the process model, wherein the process model is utilized to account for process variable variations so as to improve the defect detection accuracy.

17. The method of claim 16, wherein the defect on the at least one production semiconductor wafer is determined by identifying spatially localized abnormalities and considering process variable variations to eliminate false detections of defects.

18. The method of claim 16, further comprising calculating a difference between the obtained production wafer measurements and the calculated modeled fingerprint.

19. The method of claim 16, further comprising:

calculating a difference between obtained production wafer measurements and the calculated modeled fingerprint; and

utilizing the calculated difference when detecting the defect on the at least one production semiconductor wafer.

20. The method of claim 19, wherein the defect on the at least one production semiconductor wafer is determined by identifying spatially localized abnormalities and considering process variable variations to eliminate false detections of defects.