CLAIMS

I/We claim:

1. A wafer-level packaging assembly for light emitting diodes (LEDs), comprising:

a patterned substrate comprising a plurality of individual mounting units, wherein individual mounting units comprise a wirebond region, a first via at the wirebond region, an LED attachment site, and a second via at the LED attachment site;

an alignment substrate attached to the patterned substrate, the alignment substrate comprising a plurality of individual alignment units aligned with corresponding mounting units of the patterned substrate, and wherein the individual alignment units have a cavity exposing at least a portion of individual LED attachment sites and individual wirebond regions;

a plurality of LEDs, wherein at least one LED is positioned in each cavity, and wherein each LED has a first electric lead wirebonded to a corresponding first via in a wirebond region and a second electric lead surface mounted to a corresponding second via at an LED attachment site.

2. The packaging assembly of claim 1 wherein the patterned substrate and the alignment substrate comprise silicon substrates.

3. The packaging assembly of claim 1 wherein the patterned substrate and the alignment substrate comprise glass substrates.

4. The packaging assembly of claim 1 wherein the patterned substrate and the alignment substrate have a generally similar coefficient of thermal expansion.

5. The packaging assembly of claim 1, further comprising a converter material over at least a portion of the LED in the cavity.

6. The packaging assembly of claim 5 wherein the converter material comprises phosphor.

7. The packaging assembly of claim 1, further comprising a bonding material between the patterned substrate and the alignment substrate.

8. The packaging assembly of claim 7 wherein the bonding material comprises a metallized layer.

9. The packaging assembly of claim 7 wherein the bonding material comprises an adhesive material.

10. The packaging assembly of claim 1 wherein the wirebond region comprises a first conductive material formed on the first via on a surface of the mounting unit and the LED attachment site comprises a second conductive material formed on the second vias on the surface of the mounting unit.

11. The packaging assembly of claim 10 wherein at least one of the first or second conductive materials comprises a metallized copper structure.

12. The packaging assembly of claim 1, further comprising an electrostatic dissipation (ESD) chip near the LED.

13. The packaging assembly of claim 1 wherein the second electric lead comprises a metallized layer on a base of the LED.

14. The packaging assembly of claim 1 wherein the second electric lead comprises an N-type GaN material at the base of the LED.

15. A method for manufacturing a package for a light emitting diode (LED), the method comprising:

attaching a patterned wafer to an alignment wafer such that LED attachment sites of the patterned wafer are generally aligned with corresponding cavities of the alignment wafer;

positioning a plurality of LEDs in the cavities at the LED attachment sites by using at least one surface of the cavities to align the LEDs with the LED attachment sites; and

connecting the LEDs with wirebonding regions of the patterned wafer through wirebonds.

16. The method of claim 15, further comprising forming a phosphor converter material over at least a portion of individual LEDs in the cavities.

17. The method of claim 15, further comprising surface-mounting the LEDs to the LED attachment sites.

18. The method of claim 15, further comprising singulating the patterned wafer and the alignment wafer into a plurality of individual LED packages.

19. The method of claim 15 wherein the LEDs are electrically connected to the via through the LED attachment sites.

20. The method of claim 15 wherein attaching the patterned wafer to the alignment wafer comprises forming a bonding material of at least one of a metallization layer or an adhesive layer on at least one of the patterned wafer or the alignment wafer.

21. The method of claim 15 wherein attaching the patterned wafer to the alignment wafer comprises anodic bonding the patterned substrate to the alignment substrate.

22. The method of claim 15 wherein positioning the plurality of LEDs in the cavities comprises using at least one surface of the cavities as a mechanical stop to guide the LEDs into position on the LED attachment sites.

23. The method of claim 15 wherein the patterned wafer and the alignment wafer have generally similar coefficients of thermal expansion.

24. The method of claim 15 wherein the patterned wafer and the alignment wafer are made from at least one of silicon or glass.

25. A method for forming a packaged light emitting diode (LED), comprising:

positioning a first substrate adjacent to a second substrate, the first substrate having a plurality of mounting units and the second substrate having a plurality of alignment units, wherein individual mounting units have first vias connected to a wirebonding region and second vias connected to a LED attachment site, and wherein the individual alignment units comprise first cavities generally corresponding to the wirebonding regions of the mounting units and second cavities generally corresponding to the LED attachment sites;

attaching the first substrate to the second substrate such that the first cavities expose at least a portion of individual wirebonding regions and the second cavities expose at least a portion of individual LED attachment sites;

placing at least one LED in individual second cavities with a cathodic, conductive, base surface of the LEDs being surface-mounted to the LED attachment sites and with an anodic lead wirebonded to the wirebonding region; and

forming a phosphor converter material in the second cavities over the LEDs.

26. The method of claim 25, further comprising singulating the first and second substrates into individual packaged LEDs.

27. The method of claim 25 wherein the first substrate and the second substrate have an identical coefficient of thermal expansion.

28. The method of claim 25 wherein the first substrate and the second substrate are made from the same material.

29. The method of claim 25 wherein the wirebonding regions comprise a conductive structure formed on a surface of the first substrate, and wherein the conductive structure comprises at least one of copper, aluminum, tungsten, stainless steel, or silicon carbide.

30. The method of claim 25 wherein the LED attachment sites comprise a conductive structure formed on a surface of the first substrate, and wherein the conductive structure comprises at least one of copper, aluminum, tungsten, stainless steel, or silicon carbide.

31. A solid state lighting (SSL) device, comprising:

an LED comprising:

an N-type GaN material;

an InGaN material over the N-type GaN material; and

a P-type GaN material over the InGaN material, wherein the N-type GaN material has a conductive base through which electrical signals reach the LED;

a mounting unit with a via connected to an attachment site, the LED being surface-mounted on at least a portion of the attachment site with the conductive base connected to the attachment site;

an alignment unit positioned upon the mounting unit and attached to the mounting unit, the alignment unit having a cavity that corresponds to the attachment site, wherein the LED protrudes into at least a portion of the cavity, and wherein the mounting unit and the alignment unit have a generally similar coefficient of thermal expansion; and

a phosphor converter material formed over at least a portion of the LED in the cavity.

32. The SSL device of claim 31 wherein the conductive base comprises a metallized material on the N-type material.

33. The SSL device of claim 31 wherein:

the LED further comprises a substrate under the N-type GaN material including at least one of silicon (Si), gallium nitride (GaN), aluminum nitride (AlN), copper (Cu), aluminum (Al), tungsten (W), stainless steel (Fe), and silicon carbide (SiC);

the converter material includes a carrier material comprising at least one of a polyimide, a solvent-soluble thermoplastic polyimide, a ceramic material, and glass; and

the converter material further includes at least one of cerium(III)-doped yttrium aluminum garnet ("YAG"), neodymium-doped YAG, neodymium-chromium double-doped YAG, erbium-doped YAG, ytterbium-doped YAG, neodymium-cerium double-doped YAG, holmium-chromium-thulium triple-doped YAG, thulium-doped YAG, chromium(IV)-doped YAG, dysprosium-doped YAG, samarium-doped YAG, and terbium-doped YAG.

CLAIMS

I/We claim:

1. A wafer-level packaging assembly for light emitting diodes (LEDs), comprising:

a patterned substrate comprising a plurality of individual mounting units, wherein individual mounting units comprise a wirebond region, a first via at the wirebond region, an LED attachment site, and a second via at the LED attachment site;

an alignment substrate attached to the patterned substrate, the alignment substrate comprising a plurality of individual alignment units aligned with corresponding mounting units of the patterned substrate, and wherein the individual alignment units have a cavity exposing at least a portion of individual LED attachment sites and individual wirebond regions;

a plurality of LEDs, wherein at least one LED is positioned in each cavity, and wherein each LED has a first electric lead wirebonded to a corresponding first via in a wirebond region and a second electric lead surface mounted to a corresponding second via at an LED attachment site

and wherein the patterned substrate and the alignment substrate comprise one of a silicon substrate or a glass substrate.

2. The packaging assembly of claim 1 wherein the patterned substrate and the alignment substrate have a generally similar coefficient of thermal expansion.

3. The packaging assembly of claim 1, further comprising a converter material over at least a portion of the LED in the cavity.

4. The packaging assembly of claim 5 wherein the converter material comprises phosphor.

5. The packaging assembly of claim 1, further comprising a bonding material between the patterned substrate and the alignment substrate.

6. The packaging assembly of claim 7 wherein the bonding material comprises a metallized layer.

7. The packaging assembly of claim 7 wherein the bonding material comprises an adhesive material.

8. The packaging assembly of claim 1 wherein the wirebond region comprises a first conductive material formed on the first via on a surface of the mounting unit and the LED attachment site comprises a second conductive material formed on the second vias on the surface of the mounting unit.

9. The packaging assembly of claim 10 wherein at least one of the first or second conductive materials comprises a metallized copper structure.

10. The packaging assembly of claim 1, further comprising an electrostatic dissipation (ESD) chip near the LED.

11. The packaging assembly of claim 1 wherein the second electric lead comprises a metallized layer on a base of the LED.

12. The packaging assembly of claim 1 wherein the second electric lead comprises an N-type GaN material at the base of the LED.

13. A method for manufacturing a package for a light emitting diode (LED), the method comprising:

attaching a patterned wafer to an alignment wafer such that LED attachment sites of the patterned wafer are generally aligned with corresponding cavities of the alignment wafer;

positioning a plurality of LEDs in the cavities at the LED attachment sites by using at least one surface of the cavities to align the LEDs with the LED attachment sites;

connecting the LEDs with wirebonding regions of the patterned wafer through wirebonds; and

forming a phosphor converter material over at least a portion of individual LEDs in the cavities.

14. The method of claim 15, further comprising surface-mounting the LEDs to the LED attachment sites.

15. The method of claim 15, further comprising singulating the patterned wafer and the alignment wafer into a plurality of individual LED packages.

16. The method of claim 15 wherein the LEDs are electrically connected to the via through the LED attachment sites.

17. The method of claim 15 wherein attaching the patterned wafer to the alignment wafer comprises forming a bonding material of at least one of a metallization layer or an adhesive layer on at least one of the patterned wafer or the alignment wafer.

18. The method of claim 15 wherein attaching the patterned wafer to the alignment wafer comprises anodic bonding the patterned substrate to the alignment substrate.

19. The method of claim 15 wherein positioning the plurality of LEDs in the cavities comprises using at least one surface of the cavities as a mechanical stop to guide the LEDs into position on the LED attachment sites.

20. The method of claim 15 wherein the patterned wafer and the alignment wafer have generally similar coefficients of thermal expansion.

21. The method of claim 15 wherein the patterned wafer and the alignment wafer are made from at least one of silicon or glass.

22. A method for forming a packaged light emitting diode (LED), comprising:

positioning a first substrate adjacent to a second substrate, the first substrate having a plurality of mounting units and the second substrate having a plurality of alignment units, wherein individual mounting units have first vias connected to a wirebonding region and second vias connected to a LED attachment site, and wherein the individual alignment units comprise first cavities generally corresponding to the wirebonding regions of the mounting units and second cavities generally corresponding to the LED attachment sites;

attaching the first substrate to the second substrate such that the first cavities expose at least a portion of individual wirebonding regions and the second cavities expose at least a portion of individual LED attachment sites;

placing at least one LED in individual second cavities with a cathodic, conductive, base surface of the LEDs being surface-mounted to the LED attachment sites and with an anodic lead wirebonded to the wirebonding region; and

forming a phosphor converter material in the second cavities over the LEDs.

23. The method of claim 25, further comprising singulating the first and second substrates into individual packaged LEDs.

24. The method of claim 25 wherein the first substrate and the second substrate have an identical coefficient of thermal expansion.

25. The method of claim 25 wherein the first substrate and the second substrate are made from the same material.

26. The method of claim 25 wherein the wirebonding regions comprise a conductive structure formed on a surface of the first substrate, and wherein the conductive structure comprises at least one of copper, aluminum, tungsten, stainless steel, or silicon carbide.

27. The method of claim 25 wherein the LED attachment sites comprise a conductive structure formed on a surface of the first substrate, and wherein the conductive

structure comprises at least one of copper, aluminum, tungsten, stainless steel, or silicon carbide.

28. A solid state lighting (SSL) device, comprising:

an LED comprising:

an N-type GaN material;

an InGaN material over the N-type GaN material; and

a P-type GaN material over the InGaN material, wherein the N-type GaN material has a conductive base through which electrical signals reach the LED;

a mounting unit with a via connected to an attachment site, the LED being surface-mounted on at least a portion of the attachment site with the conductive base connected to the attachment site;

an alignment unit positioned upon the mounting unit and attached to the mounting unit, the alignment unit having a cavity that corresponds to the attachment site, wherein the LED protrudes into at least a portion of the cavity, and wherein the mounting unit and the alignment unit have a generally similar coefficient of thermal expansion; and

a phosphor converter material formed over at least a portion of the LED in the cavity.

29. The SSL device of claim 31 wherein the conductive base comprises a metallized material on the N-type material.

30. The SSL device of claim 31 wherein:

the LED further comprises a substrate under the N-type GaN material including at least one of silicon (Si), gallium nitride (GaN), aluminum nitride (AlN), copper (Cu), aluminum (Al), tungsten (W), stainless steel (Fe), and silicon carbide (SiC);

the converter material includes a carrier material comprising at least one of a polyimide, a solvent-soluble thermoplastic polyimide, a ceramic material, and glass; and

the converter material further includes at least one of cerium(III)-doped yttrium aluminum garnet ("YAG"), neodymium-doped YAG, neodymium-chromium double-doped YAG, erbium-doped YAG, ytterbium-doped YAG, neodymium-

cerium double-doped YAG, holmium-chromium-thulium triple-doped YAG, thulium-doped YAG, chromium(IV)-doped YAG, dysprosium-doped YAG, samarium-doped YAG, and terbium-doped YAG.