Method for Producing Chip Stacks as well as

a Carrier for Executing the Method

Specification

This invention relates to a method for producing chip stacks ~~as claimed in Claim 1 or 13~~ and a carrier ~~as claimed in Claim 14~~.

Due to the continuing miniaturization of structures which are present on semiconductor chips and due to existing cost pressure in mass production of semiconductor chips new methods and architectures are required to interconnect the semiconductor chips with their structures which are becoming smaller and smaller to corresponding structures on circuit boards or to adjacent chips. Here mainly the size difference of structures and connecting lines on the chip compared to conventional structures on circuit boards constitutes a technical problem. The structures of the circuit boards are also being further miniaturized and refined in order to keep up with progress in chip manufacture. Due to the existing cost pressure there is however a demand for use of more favorable circuit boards with bonding structures which have a less fine structure compared to the chip structures. This is because different types of chips, especially chips with different degrees of miniaturization, must be applied to the circuit boards so that in the production of the circuit boards as a result of further miniaturization of the bonding structures economical production would no longer be possible. Chips with a high connection density would determine the choice of circuit board material and the production process for the circuit boards.

Another technical problem is that the circuit boards of conventional design have thermal expansion which is very different from that of semiconductor materials such as silicon and

of the individual chips in the grid which however is a prerequisite for further successful processing of the hybrid wafer can also be adversely affected. For example, in the terminal the very densely packed connecting pads on the individual chips are to be bonded to contacts which are defined by means of lithography in thin film technology. Here the contacts which require the finest structure sizes are delicately most critical, therefore because the contacts which are provided directly on the chips have the finest resolution and the greatest density compared to the other layers, while the chips have the greatest variation with respect to lateral (X-Y plane) alignment accuracy. The other connecting layers, compared to the first high resolution layer with respect to lateral positioning accuracy of the individual structures, require a much smaller (factor of 2 to a factor of 5) lateral positioning accuracy than the chips.

In summary therefore the problems are as follows:

- chemical stability of the adhesives used
- thermal stability of the adhesives used
- thermomechanical stability of the adhesives used
- lack of transparency of the adhesives used (alignment accuracy)
- alignment accuracy of chips (floating)
- temperature in the detachment process

Embodiments~~Therefore the object~~ of the invention ~~is to~~ devise a method for producing chip stacks with fan-out bonding structures with which the aforementioned limitations are no longer present with respect to thermal stability, thermomechanical stability and/or chemical compatibility of the carrier with the materials used to build up the hybrid wafer and subsequent processes. Embodiments of the invention increase~~Another object consists in increasing~~ the alignment accuracy during placement and when building up the chips and

as much as possible at the same time in reducing the costs in production.

~~This object is achieved with the features of Claim 1. Advantageous developments of the invention are given in the dependent claims.~~In a first aspect, there is provided a method for producing chip stacks with the following method sequence: applying a base layer to one carrier side of a carrier which on its carrier side is provided with an adhesively acting adhesion zone and a less adhesively acting support zone, the base layer being applied by spin coating, spray coating or lamination at least largely over the entire surface of the support zone, building up the chip stacks on the base layer, wherein the base layer will at least partially get part of the chip stacks, detaching the carrier from the base layer.

In a second aspect, there is provided a method for producing chip stacks with the following method sequence: applying a base layer to one carrier side of a carrier which on its carrier side is provided with an adhesively acting adhesion zone, the base layer being applied by spin coating, spray coating or lamination over the entire surface to the adhesion zone, and one contact surface of the adhesion zone with the base layer before application of the base layer being subjected to surface modification to reduce the free surface energy, building up the chip stacks on the base layer, wherein the base layer will at least partially get part of the chip stacks, detaching the carrier from the base layer.

In a third aspect, there is provided a carrier which is provided on one carrier side with an adhesively acting adhesion zone and a less adhesively acting support zone, a base layer being applicable by spin coating, spray coating or lamination at least largely over the entire surface of the support zone, and on the carrier side, in the adhesion zone, there being a selectively soluble fill material on an offset which is set back relative to the carrier side, wherein chip stacks are built on the base layer, and wherein the base layer will at least partially get part of the chip stacks.

All combinations of at least two of the features given in the specification, the claims and/or the figures also fall within the framework of the invention. At the given value ranges, values within the indicated limits will also be disclosed as boundary values and will be claimed in any combination.

Embodiments of t~~T~~he invention are~~is~~ based on the idea of bonding the chip stacks consisting of at least one chip layer no longer directly on a carrier, but first applying to the carrier a, in particular dielectric or insulating and/or photostructurable, base layer on which in turn the chip stack is built up. Advantageously it is especially conceivable as per embodiments of~~claimed in~~ the invention for the base layer to become at least in part a component of the chip stacks or of the hybrid wafer which is to be produced. In particular, expensive temporary adhesives can be at least largely omitted.

As per embodiments of~~claimed in~~ the invention, the base layer is applied to the carrier, at least largely to a support zone with reduced adhesion force, the support zone comprising most of the area of the hybrid wafer to be produced or a large part of the area of the carrier. It is conceivable here as per embodiments of~~claimed in~~ the invention that only the one on the outermost edge of the hybrid wafer to be produced or the chip stack to be produced there is an adhesion zone with high adhesion force on the carrier [sic]. In other words: the carrier holds the base layer and the chip stacks of at least one layer of chips, which stack is to be built up on the base layer, more or less exclusively on the periphery of the base layer, the contact surface being flat between the base layer and the carrier.

The adhesion force of the adhesion zone to the base layer as per embodiments of~~claimed in~~ the invention per area is especially at least three times, preferably at least five times, even more preferably at least ten

times, ideally at least twenty times, thicker than the adhesion force of the support zone.

For the purposes of the invention the carriers can be any material suitable for producing the hybrid wafer or the piece chip stacks, especially preferred materials being those which are chosen from the groups of metal, ceramic or semiconductor, as well as quartz, glass or the like. It is also conceivable to produce a carrier consisting of a combination of these materials. The carrier can have any shape, but is advantageously square, rectangular, or especially round. One embodiment of a carrier in the shape of a round substrate with dimensions which are similar or identical to standard silicon wafers is especially advantageous, since in this case established available production machines and infrastructure can be used.

The heart of the invention therefore consists in applying a base layer to a carrier which compared to the material used for potting of the chip stack has better properties both in a chemical and also a thermal respect and in a thermomechanical respect, especially in conjunction with the detachment of the carrier from the base layer which is greatly simplified by fixing on the edge of the base layer. Both the flexibility and also the attainable alignment accuracy are greatly improved as a result of the base layer which is not potted by a layer material (molding compound). Furthermore, the production costs are improved by omitting expensive material combinations, especially with respect to temporary adhesives. Finally, and last but not least, embodiments of~~only~~ this invention makes it possible to process several chip layers into chip stacks with conductor paths which electrically connect the chips/chip stacks, especially fan-out bonding structures.

In another independent configuration as per embodiments of~~claimed in~~ the invention it is provided that the base layer can be structured by a stamping process, for example hot stamping or UV stamping methods (based on materials which can be crosslinked by irradiation by means of ultraviolet light),

especially consists of plastic, for producing chip stacks which are formed from at least one plastic chip. In this case it is conceivable that silicon can be completely omitted as per embodiments ofelaimed in the invention. The embodiment would be advantageous especially for applications in microfluidics, therefore the production of a microfluid chip and impressively shows the versatility of the method as per embodiments ofelaimed in the invention. The method step of building up the chip stacks then consists in the most general execution of this version solely in that the base layer is structured especially by a stamping method such as for example hot stamping or a UV stamping method and optionally metal coating and/or encapsulation of the structures takes place by means of a subsequent bonding method.

These stamping methods can also be used for especially economical production of electrical connections which extend through the molding compound (so-called through mold vias or TMV for short). Here the potting of the chips is carried out in a manner in which the potting tool has the desired structures, for example for producing through mold vias in the molding compound. During the potting process the potting tool is pressed into the liquid molding compound mass and the negative structures machined into the tool displace the molding compound at the intended sites. After curing of the molding compound materials, the desired positive structures remain in the cured molding compound material. In this way for example through mold vias can be produced which following a given time in the production process flow can be filled using methods conventional in the industry, especially for example electrochemical deposition of metals. This can be especially useful for applications in which for example two chip stacks which have been produced in this way are to be in turn stacked and electrically connected to one another. The TMV contacts which have been produced in the just described manner enable simple and space-saving electrically conductive

connection of the two chip stacks.

According to one advantageous embodiment of this invention it is provided that on the carrier side in the adhesion zone there is a selectively soluble fill material, especially on an offset which has been set back relative to the carrier side, preferably filling superficially flush toward the carrier side. This measure enables detachment of the carrier from the hybrid wafer or the chip stacks in an especially careful manner by the fill material being dissolved selectively by corresponding solvents which are either nonselective with respect to the other materials or which can be at least largely compartmented by it.

The described carrier can be regarded as another aspect of~~an independent~~ invention for executing the method.

By the base layer being applied to the support zone and at least in part the adhesion zone over the entire surface, the area which is available on the carrier can be used almost completely for producing the chip stacks. For a carrier diameter of 300 mm the distance, especially the ring width, from the edge of the adhesion zone to the edge of the support zone is between 0.5 mm and 10 mm, especially between 1 mm and 5 mm, preferably between 2 mm and 4 mm.

According to another advantageous embodiment of the invention, it is provided that the chip stacks are separated before detachment of the carrier, especially by cutting, so that the chip stacks are only connected to the carrier. In this case, at the same time the base layer is cut into base parts which are assigned to the chip stacks.

One embodiment is especially advantageous in which the material which forms the base layer is flexible, especially in conjunction with the measure that instead of potting with a layer material (molding compound), the material which forms the base layer is used for potting. This

additional function and by the prescribed measure the alignment accuracy of the chips/chip stacks is further increased. It is especially advantageous if the base layer is a photostructurable material, especially a photostructurable dielectric.

According to one alternative independent embodiment it is provided that the chip stacks are bonded directly onto the base layer by bonding (adhesion). This can take place either with the aid of an additional adhesive or using possible adhesive properties of the material of the base layer. Thus it is conceivable as per embodiments of~~claimed in~~ the invention for the chips to be cemented by means of a so-called die attach adhesive. Alternatively it is conceivable as per embodiments of~~claimed in~~ the invention that the material of the base layer is a dielectric which in the unexposed state largely has the behavior of a thermoplastic. Thus the chips can be fixed by means of a thermoplastic adhesive process.

It is especially advantageous if after building up the chip stacks and before detaching the carrier the chip stacks are potted, especially with a layer material which corresponds to the base layer, since in this way especially flexible and at the same time stable chip stacks or hybrid wafers can be formed.

According to another alternative embodiment of the invention it is provided that the detachment of the carrier from one side edge of the carrier, especially by reducing the adhesion force of the adhesion layer, takes place preferably by selective dissolution of the filler material. The detachment of the carrier from the base layer and the chip stack applied to the base layer, especially for the potting material, is carefully implemented by this measure as per embodiments of~~claimed in~~ the invention.

The carrier is detached from the base layer as per embodiments of~~claimed in~~ the invention by connection release means, which act especially on the adhesion zone, and the adhesion means which act in the adhesion zone between the base layer and the carrier.

solvent tank at least partially enclosing the side edge or periphery of the carrier especially effective action on the connecting layer is possible. Furthermore the measure of enclosure can prevent the fluid agent from emerging from the solvent tank or UV light intensity being lost. When using mechanical separating means possible impurities are prevented from escaping from the solvent tank and contaminating the hybrid wafer or the chip stack. The solvent tank in an advantageous configuration can be made L- or U-shaped in cross section.

The dissolution of the adhesion layer, especially of the selectively soluble filler material, can be accelerated as per embodiments of~~claimed in~~ the invention by a modulator which greatly accelerates the detachment of the carrier by means of ultrasonically or megasonically generated cavitation so that the detachment takes place much more carefully and at the same time more quickly. The modulator is in contact with the solvent used in order to ensure optimum sonic transmission. Advantageously the modulator is mechanically integrated into the L-shaped or U-shaped solvent tank. Alternatively the modulator can also be immersed into the solvent as soon as the solvent has been supplied in the intended manner for separating the adhesion layer.

Embodiments of the~~This~~ invention moreover relates to a carrier which is provided on one carrier side with an adhesively acting adhesion zone and a less adhesively acting support zone, a base layer (20) being applicable largely over the entire surface at least to the support zone, and on the carrier side in the adhesion zone there being a selectively soluble filler material, especially on an offset which is set back relative to the carrier side, preferably superficially flush with the carrier side. With a carrier which has been equipped in this way the method as per embodiments of~~claimed in~~ the invention can be carried out in an especially advantageous manner since the detachment of the hybrid wafer or the chip stack from the

carrier takes place at least largely without adversely affecting the chip stacks and the molding compound. In this way especially careful detachment of the expensive chip stack is ensured. Moreover it is conceivable as per embodiments of~~claimed in~~ the invention to interconnect several adjacent chip stacks when the chip stacks are built up and/or the fan-out bonding structures are formed into chip stack structures (see embodiment F).

It is furthermore advantageously provided that the detachment of the carrier takes place concentrically from the periphery of the carrier to the center of the carrier.

Other advantages, features and details of the invention will become apparent from the following description of preferred exemplary embodiments and using the drawings,

Figures 1A to 1E, 9F1, 10G1 and 11H1 show a schematic view of a step of application of a base layer to a carrier as claimed in the invention according to embodiments A to H,

Figures 2A to 2E and 11H2 show a schematic view of a step of introducing fan-out bonding structures and alignment marks into the base layer as claimed in the invention according to embodiments A to E and H,

Figures 3A to 3E and 11H3 show a schematic view of a step of placing contact pads on the base layer as claimed in the invention according to embodiments A to E and H,

Figures 4A to 4E, 9F2, 10G4 and 11H4 show a schematic view of a step of stacking chips onto the base layer in at least one position as claimed in the invention according to embodiments A through H,

Figures 5A to 5E, 10G5 and 11H5 show a schematic view of a step of potting the chips stacks with molding compound as claimed in the invention according to embodiments A to E, G and H,