CLAIMS

1. A method for manufacturing a semiconductor-on-insulator integrated circuit chip comprising the following steps:
a) providing a semiconductor-on-insulator structure (100) having a buried insulating layer (2) which is sandwiched between a support substrate (1) and a top semiconductor-containing layer (3), said top semiconductor-containing layer (3) having a first thickness, comprised between 20nm and 80nm, throughout the semiconductor-on-insulator structure (100), then
b) building a plurality of field effect transistors (110,120), wherein each field effect transistor is isolated from the others and comprises:
- a preliminary gate (31,32) above a channel region (30) of the top semiconductor-containing layer (3), the field effect transistors (110,120) from a first group having a first preliminary gate length and the field effect transistors (120) from a second group having a second preliminary gate length smaller than the first one,
- a source region (40) and a drain region (50) formed by n-type or p-type dopant implantation in the top semiconductor-containing layer (3), and extending down to the buried insulating layer (2),
- a source electrode (41,42) and a drain electrode (51,52) respectively on the source region (40) and the drain region (50), then
c) removing at least the preliminary gates (32) of the field effect transistors (120) from the second group, leaving access to the channel regions (30) of said field effect transistors (120), then
d) thinning the top semiconductor-containing layer (3) in channel regions of the field effect transistors (120) from the second group, so as to reach a second thickness,

comprised between 4nm and 20nm, wherein the top semiconductor-containing layer (3) in channel regions (30) of the field effect transistors (110) from the first group has the first thickness, then

e) forming functional gates (72) simultaneously on channel regions (30’) of the field effect transistors (120) whose preliminary gate (32) was removed,

wherein a chip comprises at least one field effect transistor (110) from the first group and at least one field effect transistor (120) from the second group,

wherein the field effect transistors (110) of the first group are high voltage analog, RF and/or I/O devices, and the field effect transistors (120) of the second group are low voltage digital and/or RF devices.

2. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to the preceding claim, wherein the step c) comprises removing the preliminary gates (31) of the field effect transistors (110) from the first group, leaving access to the channel regions (30) of said field effect transistors (110).

3. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the step of thinning comprises a two-stages etch, a first etch up to 1nm to 5nm of the second thickness, and a second etch with slow etching rate to reach the second thickness.

4. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to claim 3, wherein the first etch is based on anisotropic dry etching.

5. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of claims 3 and 4, wherein the second etch is based on wet or dry etching, or atomic layer etching, with a etch rate lower than 1 nm/min.

6. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the second thickness is equal to a quarter of a length of a gate electrode of the field effect transistor (FET) devices (120) from the second group.

7. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the buried insulating layer (2) has a thickness comprised between 10nm and 50nm.

8. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the step a) of building a plurality of field effect transistors (110,120) comprises, before the formation of the preliminary gates (31,32), a formation of back gates under the buried insulating layer (2), in the support substrate (1), opposite to the subsequently formed preliminary gates (31,32) of the field effect transistors (110,120) from the first group and/or from the second group.

9. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the field effect transistors (110,120) are based on planar or 3D or finFET device architectures.

10. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the step d) comprises thinning the top

semiconductor-containing layer (3) in channel regions of field effect transistors from a third group, so as to reach a third thickness, different from the second thickness, and wherein the step e) comprises forming the same functional gate on each channel region of the field effect transistors from the third group, wherein a chip comprises at least one field effect transistor from the third group.

11. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the top semiconductor-containing layer (3) comprises at least one material among silicon, silicon germanium, silicon carbide, III-V compounds or gallium nitride.

12. The method for manufacturing a semiconductor-on-insulator integrated circuit chip according to any of the preceding claims, wherein the support substrate (1) comprises monocrystalline and/or poly-crystalline silicon, or a combination of other semiconductor materials.