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A DIGITAL MULTIPLIER WITH REDUCED SPURIOUS SWITCHING BY MEANS OF LATCH ADDERS

Field of the Invention

[0001] This invention relates to a Multiplier, and particularly to a digital Parallel Multiplier to reduce spurious switching by means of Latch Adders, thereby reducing the power dissipation.

Background of the Invention

[0002] Many advanced existing electronic devices employ a digital signal processor (DSP) to perform complex signal processing. Most digital signal processing functions require multiplication that is realized by a Multiplier, addition that is realized by an Adder, subtraction that is realized by an Adder (with simple modifications to the inputs) and in some special applications, division that is realized by a divider. All these mathematical operations involve addition that is realized by an Adder. In typical mathematically intensive computations, the power dissipated by the DSP is usually dominated by the Multiplier.

[0003] It is well established that the primary power dissipation mechanism of the Multiplier is the dynamic switching power that is due to the large number of high speed transistor switching on and off within the Multiplier. This switching power problem is well recognized within the electronics industry. Generally, it is desirable that the power dissipation be as low as possible as this leads to a longer battery life for portable devices, less heat dissipation problems, etc. A well-established method to reduce the power dissipation of Multipliers is to reduce spurious switching (unnecessary transistor switching) where possible.

[0004] Multipliers may be categorized into two general classes: Serial and Parallel Multipliers. Parallel Multipliers are more popular as they have improved speeds over Serial Multipliers and they often dissipate lower power. However, their

integrated circuit (IC) area requirement is usually larger but this is not usually a problem.

[0005] A Parallel Multiplier generally comprises three functional blocks as shown in FIG. 1. A Multiplicand input (X) 1 and a Multiplier input (Y) 2 are entered into a Partial Product Generator functional block 3 and the Partial Product Generator 3 generates partial products. The Partial Product Generator 3 can be realized by different methodologies including the Radix-2 algorithm, Booth algorithm, modified Booth algorithm, Baugh-Wooley algorithm, etc. The partial products are subsequently added in the First Stage Adder Circuit 4 whose internal structure is usually either array-based or tree-based. A Multiplier whose First Stage Adder Circuit 4 is based on an array structure is henceforth termed a Parallel Array Multiplier, and a Multiplier whose First Stage Adder Circuit 4 is based on a tree structure is henceforth termed a Parallel Tree Multiplier. The design of Parallel Multipliers is well established and is described in a book authored by Wakerly entitled *Digital Design - Principles & Practices*, 3rd Edition, Prentice Hall, 2000 (Wakerly). The most popular tree-based structure is the Wallace-Tree, first proposed by Wallace in, "A Suggestion for a Fast Multiplier," *IEEE Transactions on Electronic Computers*, vol. 13, pp. 14-17, Feb. 1964. The adders in the First Stage Adder Circuit 4 can be realized by a number of different adders including the Carry-Ripple Adder, Carry-Save Adder, Carry-Look-ahead Adder, etc, and the Carry-Save Adder is probably the most popular design. An Adder 7 in the First Stage Adder Circuit 4 can be a Full Adder (FA), a Half Adder (HA) or a combination of these simple adders. Wakerly gives a good description of these prior-art adders. A first subscript 8 and a second subscript 9 of the Adder 7 respectively denote a row and a column of the Adder 7. As an illustration in FIG. 1, there are M rows of Adders 7 in the First Stage Adder Circuit 4. The number of columns in each row may be different depending on specific Parallel structure. In the first row 10 there are a columns 13, in the second row 11 there are b columns 14, ..., and in the M^{th} row 12, there are z columns 15. It is well known that the number of adders 7 in this First Stage Adder Circuit 4 of a Parallel Array Multiplier

is essentially the same for all rows. It is also well known that the number of rows of Adders 7 in the First Stage Adder Circuit 4 of a Parallel Tree Multiplier is less (than that in the Parallel Array Multiplier) and that the number of adders reduces from the first row to the last row. Consequently, the Parallel Tree Multiplier is usually faster (than the Parallel Array Multiplier) and potentially dissipates less power. However, its layout structure is less regular.

[0006] The output of the First Stage Adder Circuit 4 comprising the partial product additions goes to the Final Stage Adder Circuit 5. The Final Stage Adder Circuit 5 is usually one row of adders. Usually, the output of the Final Stage Adder Circuit 5 and some products from the First Stage Adder Circuit 4 collectively forms the Multiplication Product 6.

[0007] The abovementioned spurious switching primarily occurs in internal nodes of the First Stage Adder Circuit 4 and in internal nodes of the Final Stage Adder Circuit 4. The origin of the spurious switching in the First Stage Adder Circuit 4, and in the Final Stage Adder Circuit 4, may be attributed to the different arrival times of input signals to the different adders. In the First Stage Adder Circuit 4, the spurious switching propagates from nodes in input stages of the first row to the latter rows where the amount of spurious switching usually increases substantially. Typically, the amount of spurious switching in the Final Stage Adder Circuit 5 is substantially less than that in the First Stage Adder Circuit 4, because the Final Stage Adder Circuit 5 usually comprises a significantly smaller number of adders. However, the amount of spurious switching per adder in the Final Stage Adder Circuit 5 may be higher.

[0008] Several methods have been proposed to reduce undesired spurious switching. For example, US patent 5,333,119 Raatz et al. employs a delayed-evaluation technique where delay lines are used to appropriately time the turning on/off of dynamic CMOS adders in the First Stage Adder Circuit 4. However, because the dynamic CMOS adders require constant pre-charging and evaluation of

output logic levels according to applied inputs, the adders potentially feature higher spurious switching activity compared to more conventional static CMOS adders. In US patent 5,787,029 de Angel, a logic called an Enable/Disable CMOS Differential Logic (ECDL) is applied. The ECDL is used to construct computation units including basic adder cells that operate in an iterative manner in the First Stage Adder Circuit 4. This operation potentially reduces intermediate spurious switching in Multipliers. However, as such ECDL adders require reset and enable operations (similar to that of the dynamic CMOS adders) to appropriately time the turning on/off of the ECDL adders, the advantages gained are mitigated by potentially higher spurious switching activity. Furthermore, the ECDL adders require complementary signals that double switching activity and require a larger IC area. Yet another method to reduce undesired spurious switching is described in US Patent 5,818,743 Lee et al, which places a plurality of delay elements and registers in selected signal lines to delay arrival of signals to a Booth Encoder in the Partial Product Generator 3 and to the adders in the First Stage Adder Circuit 4 and this thereby improve synchronicity of input timings. These delay elements and registers are circuits form separate circuit entities that are independent of the adders and Encoder. As these delay elements, registers and adders are separate circuit entities, the added hardware costs are high because of the additional delay elements and registers. Furthermore, additional power costs from the delay elements and registers may instead increase overall power dissipation of the Multiplier rather than reducing power dissipation originally obtained from reduced spurious switching. In summary, the abovementioned methods attempt to reduce spurious switching by appropriately timing the input signals such as by delaying. However, overheads for realizing these timing adjustments are high and may defeat the advantages of reduced spurious switching.

[0009] Lemonds et al., in a technical paper entitled “A Low Power 16 by 16 Multiplier Using Transition Reduction Circuitry,” *International Workshop on Low Power Design*, pp. 139-142, April 1994 (Lemonds 1994), proposes placing latches at the input (in front) of the adders in the First Stage Adder Circuit 4 and clocking

the latches in a precise sequence so that inputs to the adders are synchronized. Although the spurious switching is reduced, the overhead cost of the latches remains high. This is because the latches are circuit entities independent of (and separate from) the adders, as in US Patent 5,818,743 Lee et al. Thus, the power savings from reduced spurious switching may be offset by power dissipation of the latches that are external to the adders. Furthermore, circuit costs of these latches in terms of IC area may also be high to eliminate or reduce advantages of reduced spurious switching described in Lemonds 1994.

[0010] Jou et al., in a technical paper entitled “A 200-MHz CMOS Pipelined Multiplier-Accumulator Using a Quasi-Domino Dynamic Full-Adder Cell Design,” *IEEE Journal of Solid-State Circuits*, vol. 28, No. 2, pp. 123-132, Feb. 1993 (Jou 1993), proposes to include a CMOS dynamic Latch at the output of all adders to perform logic inversion, buffering and pipelining functions. The objective of this proposal was to increase throughput rate of the Multiplier. Although this design indirectly reduces spurious switching in subsequent stages of the adders in the First Stage Adder Circuit 4, the reduction of the spurious switching may not be significant for two reasons. First, with the latch placed at the output instead of the input, some spurious switching does occur within the adder. Second, because not all the outputs of the adders in one row are connected to the input of the following row of adders (in particular in Tree-based First Stage Adder Circuits), but instead are also connected to the inputs of some adders in other rows, substantial spurious switching may still occur in the adders of these other rows. In short, there remains substantial spurious switching in the proposal described in Jou 1993.

[0011] All the abovementioned methods or proposals are intended for synchronous digital logic circuits only and their application to asynchronous logic circuits is uncertain. A good description of synchronous logic circuits and asynchronous logic circuits can be found in a book authored by Tinder and entitled *Digital Engineering Design – A Modern Approach*, Prentice-Hall, 1991.

[0012] Hence, it would be highly desirable to have synchronous logic-based and/or asynchronous logic-based Parallel Multipliers with reduced spurious switching in the First Stage Adder Circuit 4 and/or with reduced spurious switching in the Final Stage Adder Circuit 5 wherein the reduced spurious switching in the First Stage Adder Circuit 4, and/or Final Stage Adder Circuit 5 is obtained with little overhead costs resulting from a small amount of added hardware dissipating less power than existing or prior art methods or proposals.

Summary of the Invention

[0013] The present invention seeks to provide synchronous logic and asynchronous logic Multiplier Circuits with reduced spurious switching, and the overhead cost for realizing the reduced spurious switching is low.

[0014] Accordingly, in one aspect, the present invention provides a digital Multiplier having a Partial Product Generator, a First Stage Adder Circuit and a Final Stage Adder Circuit, wherein the First Stage Adder Circuit comprises at least one Latch Adder, at least one of the Latch Adder comprising at least one Latch being an integral part thereof.

[0015] In another aspect, the present invention provides a digital Multiplier having a Partial Product Generator, a First Stage Adder Circuit and a Final Stage Adder Circuit, wherein the Final Stage Adder Circuit having at least one Latch Adder, at least one of the Latch Adder comprising at least one Latch being an integral part thereof.

[0016] In a further aspect, the present invention provides a Latch Adder comprising at least one Latch and at least one Adder, at least one of the Latch being integrally formed with at least one of the Adder.

Brief Description of the Drawings

[0017] Embodiments of the present invention shall now be more fully described, by way of examples, with reference to the drawings of which:

[0018] FIG. 1 is a block diagram of a prior-art general Parallel Multiplier based on synchronous logic;

[0019] FIG. 2 is a block diagram of a Prior-art Full Adder; and

[0020] FIG. 3 is a block diagram of a Prior-art Full Adder with a Latch at each of its inputs;

[0021] FIG. 4a is a block diagram of a Latch Adder in which a Latch Circuit Block overlaps an Adder Circuit Block to depict a Latch being an integral part of an Adder in accordance with the invention;

[0022] FIG. 4b is a simplified block diagram of the Latch Adder of FIG. 4a;

[0023] FIG. 4c is a circuit schematic of the Latch Adder of FIG. 4a in accordance with one alternate embodiment;

[0024] FIG. 4d is a circuit schematic of the Latch Adder of FIG. 4a in accordance with a preferred embodiment;

[0025] FIG. 4e is a circuit schematic of the Latch Adder of FIG. 4a in accordance with another alternate embodiment;

[0026] FIG. 5 is a circuit schematic of a Control Circuit of the Latch Adder of FIG. 4a;

[0027] FIG. 6 is a general block diagram of a synchronous logic Parallel Multiplier with reduced spurious switching in accordance with the present invention; and

[0028] FIG. 7 is a block diagram of a general asynchronous logic Parallel Multiplier with reduced spurious switching in accordance with the present invention.

Detailed Description of the Drawings

[0029] FIG. 2 depicts a block diagram of a prior-art adder 7 of the First Stage Adder Circuit 4 of a Parallel Multiplier. As described earlier, this prior-art adder 7 is usually a Carry-Save Adder. Inputs to the adder 7 are a partial product A_{21} , a

partial product B 22, and a Carry-in (C_{in}) 23. Outputs from the adder 7 are Sum (S) 24 and Carry-out (C_{out}) 25. The subscripts i and x of the adder 7 respectively denote an i^{th} row and an x^{th} column of the First Stage Adder Circuit 4.

[0030] As described earlier, it is well established that spurious switching in the First Stage Adder Circuit 4 and/or the Final Stage Adder Circuit 5 may be reduced by synchronizing the inputs to the adders in each row. It was also described earlier that several existing methods or proposals have attempted to achieve this synchronization by means of latches or other logic circuits with similar functions. Generally, most of these existing methods or proposals are shown in FIG. 3 where the latches 31 are asserted by the Latch Control Signal 32 to simultaneously latch the inputs A 21, B 22 and C_{in} 23 to thereby synchronize the inputs. However, as these latches or other similar logic circuits are independent of (separate from) the adders, that is the latches and the adder are separate circuit entities, their added overhead cost to the Multiplier in terms of additional hardware and added power dissipation may be exorbitant. Put differently, the additional hardware and added power dissipation costs may instead offset advantages gained by reduced spurious switching.

[0031] The present invention circumvents the abovementioned costs by placing the latch function as an integral part of the adder and these adders are henceforth termed Latch Adders, abbreviated as LA. This is pictorially shown in FIG. 4a in which the Latch Circuit Block overlaps the Adder Circuit Block, depicting that the Latch 42 is an integral part of the Adder 43. The Latch 42 is asserted by means of the Latch Control Signals 44 and the inputs to the Adder 43 within the Latch Adder are therefore made to arrive (into the Adder 43) at the same time. In other words, the input signals are now synchronized. In FIG. 4a, the Latch Circuit Block is shaded with left leaning lines, the Adder Circuit Block is shaded with right leaning lines, and the overlap is shaded by cross-hatching. This pictorial diagram can be simplified into the Latch Adder block depicted in FIG. 4b where the Latch 42, integrated with the Adder 43, is asserted by means of the Latch Control Signals 44.

By making the Latch 42 function an integral part of the Adder 43, as opposed to the Latch 42 and the Adder 43 being separate circuit entities, the power dissipation of the Latch Adder 41 is only marginally higher than existing prior-art Adders, and the circuit hardware cost is also only marginally higher. However, the full advantages of the spurious switching reduction are retained upon synchronizing the input signals. Put differently, by means of placing the Latch 42 function as an integral part of the Adder 43 function, the power dissipation (due to reduced spurious switching) may be substantially reduced and the added cost is small. It is to be noted that as the Latch 42, integrated with the Adder 43, is effectively in the front of the Latch Adder 41, there is little, if any, spurious switching within the Latch Adder 41. This is another important difference between the present invention and that proposed by Jou 1993 in which a latch was placed at the output of an adder.

[0032] Placing the Latch 42 within the Adder 43 is, in some sense, akin to placing (cache) memory within a microprocessor. Traditionally, a microprocessor accesses memory that is external to the microprocessor and the disadvantage of this is the slower memory access and higher power due to the long interconnections between the microprocessor and the memory. By placing some memory as an integral part of the microprocessor, called the cache memory, memory access is faster and with lower power dissipation due to reduced interconnections. In other words, the advantages are obtained only when the cache memory is an integral part of the microprocessor and not the case when the memory and microprocessor are separate circuit entities.

[0033] By appreciating that it is advantageous to place the Latch 42 as an integral part of the Adder 43, a person skilled in the art can design a Latch Adder 41 in a number of ways. For example, FIG. 4c shows one alternate embodiment of the Latch Adder 41. When the control transistors 45,46,47,48,49,50 are asserted by the Latch Control Signals SG_i and $\overline{SG_i}$ 44, the Latch Adder 41 functions as a Full Adder whose inputs are A 21, B 22 and C_{in} 23 and outputs are S 24 and C_{out} 25.

When control transistors 45,46,47,48,49,50 are negated (de-asserted) by the Latch Control Signals SG_i and $\overline{SG_i}$ 44, the input signals A 21, B 22 and C_{in} 23 are blocked and ignored by the Latch Adder 41 and the states of the previous S 24 and C_{out} 25 signals are respectively retained by means of inverter 51 and inverter 52. A person skilled in the art can easily redesign this Latch Adder 41 that functions as a Full Adder shown FIG. 4c to another Latch Adder that functions as a Half Adder or any combination of Full and Half Adders.

[0034] It is reiterated that by appreciating the advantages of placing the Latch 42 as an integral part of the Adder 43, a person skilled in the art can design a Latch Adder 41 with the Latch 42 as an integral part of the Adder 42 in a number of ways. For example, FIG. 4d depicts the preferred embodiment of the invention. When the control transistors 53, 54, 55, 56 are asserted by the Latch Control Signals SG_i and $\overline{SG_i}$ 44 the Latch Adder 41 functions as a Full Adder whose inputs are A 21, B 22 and C_{in} 23 and outputs are S 24 and C_{out} 25. When control transistors 53, 54, 55, 56 are negated (de-asserted) by the Latch Control Signals SG_i and $\overline{SG_i}$ 44 the input signals A 21, B 22 and C_{in} 23 are blocked, that is ignored by the Latch Adder 41 and the states of the previous S 24 and C_{out} 25 signals are respectively retained by means of inverter 57 and inverter 58. As in the alternate embodiment of the invention shown in FIG. 4c, a person skilled in the art can easily redesign this Latch Adder 41 that functions as a Full Adder shown FIG. 4d to another Latch Adder that functions as a Half Adder or any combination of Full and Half Adders.

[0035] It is again to be reiterated that by appreciating the advantages of placing the Latch 42 as an integral part of the Adder 43, a person skilled in the art can design a Latch Adder 41 with the Latch 42 as an integral part of the Adder 43 in a number of ways. For example, FIG. 4e depicts another alternate embodiment of the invention. When the control transistors 59,60,61,62, are asserted by the Latch Control Signals SG_i and $\overline{SG_i}$ 44, the Latch Adder 41 functions as a Full Adder

whose inputs are A 21, B 22 and C_{in} 23 and outputs are S 24 and C_{out} 25. When control transistors 59,60,61,62, are negated (de-asserted) by the Latch Control Signals SG_i and $\overline{SG_i}$ 44 the input signals A 21, B 22 and C_{in} 23 are blocked, that is ignored by the Latch Adder 41 and the states of the previous S 24 and C_{out} 25 signals are respectively retained by means of inverter 63 and inverter 64. As in the preferred and alternate embodiments of the invention, a person skilled in the art can easily redesign this Latch Adder 41 that functions as a Full Adder shown FIG. 4e to another Latch Adder that functions as a Half Adder or any combination of Full and Half Adders.

[0036] As discussed, the Latch Control Signals 44 control the synchronization of the inputs A 21, B 22 and C_{in} 23 by means of the Latches within the Latch Adder 41. FIG. 5 is a circuit schematic of the Latch Control Circuit 71. This Control Circuit 71 serves two purposes – it generates the Latch Control Signals SG_i and $\overline{SG_i}$ 44 and it functions as a delay circuit. The function of the Latch Control Signals 44 has been described hereinabove. The function of the delay circuit is to provide a delay that is equal in duration to the longest time for the Latch Adder 41 in the preceding row to complete its addition of inputs A 21, B 22 and C_{in} 23 and to output S 24 and C_{out} 25. In this manner, the inputs A 21, B 22 and C_{in} 23 to all the Latch Adders 41 in the subsequent row are synchronized in time, thereby reducing the spurious switching. It is well known that the duration of the delay of the Control Circuit 71 comprising a number of inverters is determined by the number of inverters 72 and by the aspect ratio of the transistors in these inverters 72. A person skilled in the art can design the Control Circuit 71 in a number of ways, including using other types of logic gates.

[0037] FIG 6 is a general block diagram of a synchronous logic Parallel Multiplier for the preferred and alternate embodiments of the invention. This general block diagram encompasses both the Parallel Array Multiplier and the Parallel Tree Multiplier where their respective First Stage Adder Circuit 81 is an array-based structure and a tree-based structure. In the First Stage Adder Circuit 81 the Adders

(usually Carry-Save Adders) in the First Stage Adder Circuit of prior-art adders 7 in FIG 1, are now replaced by Latch Adders 41. Each of the Latch Adders 41 in the same i^{th} row may be controlled by the same Latch Control Signals SG_i and $\overline{SG_i}$ 44 for $1 \leq i \leq M$, where M is the number of rows in the First Stage Adder Circuit 81. The Control Circuit 71 in the first row, is activated by Control Signal 83, which is usually the active clock edge of the synchronous clock signal. When the Control Circuits 71 assert Latch Control Signals 44, the Latch Adders 41 in the same row are activated and the addition processes for that row are simultaneously initiated. In other words, the timing of the different input signals A 21, B 22 and C_m 23 to all Latch Adders 41 in the row is thereby synchronized. When the Control Circuits 71 negate the Latch Control Signals 44, all the Latch Adders 41 in that row ignore their inputs and hold their previous states. The output of all Latch Adders 41 in that row remain unchanged, and the input signals to the adders in the row immediately below the row or inputs of other rows connected to any output of Latch Adders 41 in that row also remain unchanged. Consequently, the spurious switching is substantially reduced because the Latch Adders 41 synchronize the timing of their inputs by means of the Latch Control Signals 44. As the Latch Adders 41 require only one switching in each operation, they therefore dissipate substantially lower power than the prior-art dynamic CMOS adders and ECDL adders. This is because, as previously discussed, prior-art dynamic CMOS adders and ECDL adders usually require more than one switching for each operation. It is reiterated that the substantial power savings from the invention is marginally reduced due to the power dissipation of the Control Circuits 71 and the slight increase in power dissipation of the Latch Adders 41 over the conventional prior-art Adder 7 that is usually the Carry-Save Adder. For 16x16 bit Multipliers whose Partial Product Generator 3 is based on the Booth algorithm, the overall power saving of the synchronous logic Parallel Multiplier embodying the invention is of the order of 30% over prior-art conventional 16x16 bit synchronous logic Parallel Multipliers. This overall magnitude of the power saving differs for other 16x16 bit Multipliers whose Partial Product Generator 3 is based on different methodologies. The overall magnitude of the power saving is more substantial for larger Multipliers, for

example 32x32 bit Parallel Multipliers. This invention can also be applied to the Final Stage Adder Circuit 82 to reduce the spurious switching. This latter application may, however, reduce the overall speed of the Multiplier.

[0038] It is possible to further improve the power savings of a Parallel Multiplier embodying the invention for synchronous logic by strategically placing the Latch Adders 41 and the Control Circuits 71 in the First Stage Adder Circuit 81 instead of simply placing the Latch Adders 41 and the Control Circuits 71 in every row as described earlier. One improvement is to replace the conventional adders 7 with Latch Adders 41 and place the Control Circuit 71 only from the second row to the last row in the First Stage Adder Circuit 81. Another improvement would be to replace the conventional adders 7 with Latch Adders 41 and place the Control Circuit 71 only in the odd rows of the First Stage Adder Circuit 81.

[0039] It should be clear that a person skilled in the art can easily apply the invention to a Parallel Multiplier based on asynchronous logic. FIG. 7 is a block diagram of such an asynchronous logic Parallel Multiplier. An asynchronous logic Parallel Multiplier typically requires two signals in addition to those required by conventional synchronous logic Multipliers. These signals usually include the Request (REQ) signal 93 and Acknowledge (ACK) signal 94 and these signals serve as handshaking signals. In this example, the First Stage Adder Circuit 91 comprises rows embodying the Latch Adders 41 and Control Circuits 71. The workings of the First Stage Adder Circuit 91 of this asynchronous logic Parallel Multiplier is similar to that of the synchronous logic Parallel Multiplier abovementioned. The REQ signal 93 is asserted after the input Multiplicand X 1 and Multiplier Y 2 signals have arrived. The ACK signal 94 at the output of the asynchronous Final Stage Adder Circuit 92 is asserted to indicate the completion of the multiplication process. The spurious switching in the First Stage Adder Circuit 91 may be substantially reduced by replacing the prior-art conventional adders with Latch Adders 41. Similarly, the adders in the Final Stage Adder Circuit 92, may also be replaced with Latch Adders 41 to reduce the spurious switching.

[0040] It should be clear that a person skilled in the art can design the Latch Adders 41 in a number of ways wherein the Latch 42 is an integral part of the Adder 43 and are not separate circuit entities. It should be also be clear that the Latch Adder 41 described herein can be applied in many logic circuit applications, including as a stand-alone Adder, a stand-alone Subtractor (realized with simple modifications to the inputs of the Latch Adder 41), in Multipliers, Dividers, etc. It should also be clear that a person skilled in the art can design a Parallel Multiplier by using a number of different methodologies for realizing the Partial Product Generator 3 including Radix-2 algorithm, Booth algorithm, modified Booth algorithm, Baugh-Wooley algorithm, etc, and with the First Stage Adder Circuit, embodying Latch Adders 41. The different methodologies may further include a First Stage Adder Circuit whose rows may be increased or decreased and the number of adders in the rows may also be increased or decreased when compared to the examples given herein. It should also be clear that a person skilled in the art can design a Parallel Multiplier using a number of different designs for realizing the Final Stage Adder Circuit including the Carry-Ripple Adder, Carry-Look-ahead Adder, Carry-Skip Adder, etc, and replacing any of these prior-art adders with a Latch Adder 41. It should further be clear that a person skilled in the art can design the Latch Control Circuit described herein in a number of different ways, and design the Latch Control Signals to be generated in a number of different ways, including without the need for a specific Control Circuit, and simplify the Control Signals from a differential signal to a single-ended signal. It should yet further be clear that a person skilled in the art can design both unsigned and signed Multipliers embodying the invention.

[0041] Having described the above embodiments with reference to the accompanying drawings, it is to be understood that the invention is not limited to these embodiments and that various changes and modifications can be made by one skilled in the art without departing from the spirit and scope of the novel concepts of the invention as defined in the appended claims.

Claims

1. A digital Multiplier having a Partial Product Generator, a First Stage Adder Circuit and a Final Stage Adder Circuit, wherein said First Stage Adder Circuit comprises at least one Latch Adder, wherein at least one of said Latch Adder comprises at least one Latch being an integral part thereof.
2. A digital Multiplier set forth in Claim 1, wherein said at least one of said Latch Adder latches at least one input signal to said at least one of said Latch Adder.
3. A digital Multiplier set forth in Claim 2, wherein at least two input signals of said input signal to said at least one of said Latch Adder are synchronized by means of said at least one of said Latch.
4. A digital Multiplier set forth in Claim 3, wherein said at least two input signals reduces spurious switching upon synchronizing.
5. A digital Multiplier set forth in Claim 1, wherein said at least one of said Latch Adder is controlled by at least one Control Signal.
6. A digital Multiplier set forth in Claim 5, wherein said at least one of said Control Signal is generated by at least one Control Circuit.
7. A digital Multiplier set forth in Claim 6, wherein said at least one of said Control Circuit is a Delay Circuit.
8. A digital Multiplier set forth in Claim 1, wherein at least one row in said First Stage Adder Circuit comprises said at least one of said Latch Adder.
9. A digital Multiplier having a Partial Product Generator, a First Stage Adder Circuit and a Final Stage Adder Circuit, wherein said Final Stage Adder Circuit comprises at

least one Latch Adder, wherein at least one of said Latch Adder comprises at least one Latch being an integral part thereof.

10. A digital Multiplier set forth in Claim 9, wherein said at least one of said Latch Adder latches at least one input signal to said at least one of said Latch Adder.
11. A digital Multiplier set forth in Claim 10, wherein at least two input signals of said input signal to said at least one of said Latch Adder are synchronized by means of said at least one of said Latch.
12. A digital Multiplier set forth in Claim 11, wherein said at least two input signals reduces spurious switching upon synchronizing.
13. A digital Multiplier set forth in Claim 9, wherein said at least one of said Latch Adder is controlled by at least one Control Signal.
14. A digital Multiplier set forth in Claim 13, wherein said at least one of said Control Signal is generated by at least one Control Circuit.
15. A digital Multiplier set forth in Claim 14, wherein said at least one of said Control Circuit is a Delay Circuit.
16. A Latch Adder comprising at least one Latch and at least one Adder, wherein at least one of said Latch is integrally formed with at least one of said Adder.
17. A Latch Adder set forth in Claim 16, wherein said at least one of said Latch latches at least one input signal to said at least one of said Adder.
18. A Latch Adder set forth in Claim 16, wherein said at least one of said Latch is controlled by at least one control signal.

19. A Latch Adder set forth in Claim 16, wherein at least two input signals to said at least one of said Latch Adder are synchronized by means of said at least one of said Latch.
20. A Latch Adder set forth in Claim 19, wherein said at least two input signals reduces spurious switching upon synchronizing.