CLAIMS

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits;

patterning the mask with a multiple pass laser scribing process to provide a patterned mask with gaps exposing regions of the semiconductor wafer between the integrated circuits, the multiple pass laser scribing process comprising a first pass along a center scribing path, a second pass along a first edge scribing path, a third pass along a second edge scribing path, a fourth pass along the second edge scribing path, a fifth pass along the first edge scribing path, and a sixth pass along the center scribing path, wherein the first pass is performed prior to the second pass, the second pass is performed prior to the third pass, the third pass is performed prior to the fourth pass, the fourth pass is performed prior to the fifth pass, and the fifth pass is performed prior to the sixth pass; and

plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits.

2. The method of claim 1, wherein the multiple pass laser scribing process comprises using a laser beam having a spot size of approximately 10 microns.

3. The method of claim 2, wherein a spacing between centers of the first edge scribing path and the center scribing path is approximately 5 microns, and a spacing between centers of the center scribing path and the second edge scribing path is approximately 5 microns.

4. The method of claim 3, wherein patterning the mask with the multiple pass laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, and wherein the trenches have a width of approximately 20 microns and a depth in the range of 5-6 microns.

5. The method of claim 2, wherein a spacing between centers of the first edge scribing path and the center scribing path is approximately 8 microns, and a spacing between centers of the center scribing path and the second edge scribing path is approximately 8 microns.

6. The method of claim 5, wherein patterning the mask with the multiple pass laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, and wherein the trenches have a width in the range of 25 to 30 microns and a depth of 5 microns or less.

7. The method of claim 1, wherein the multiple pass laser scribing process is based on a Gaussian laser beam.

8. The method of claim 1, wherein the multiple pass laser scribing process is based on a line-shaped laser beam having a flat top.

9. A system for dicing a semiconductor wafer comprising a plurality of integrated circuits, the system comprising:

a factory interface;

a laser scribe apparatus coupled with the factory interface and comprising a laser assembly configured to provide a multiple pass laser scribing process comprising multiple passes along a first edge scribing path, multiple passes along a center scribing path, and multiple passes along a second edge scribing path, wherein the laser assembly is configured to provide the multiple pass laser scribing process comprising a first pass along the center scribing path, a second pass along the first edge scribing path, a third pass along the second edge scribing path, a fourth pass along the second edge scribing path, a fifth pass along the first edge scribing path, and a sixth pass along the center scribing path, and wherein the first pass is performed prior to the second pass, the second pass is performed prior to the third pass, the third pass is performed prior to the fourth pass, the fourth pass is performed prior to the fifth pass, and the fifth pass is performed prior to the sixth pass; and

a plasma etch chamber coupled with the factory interface.

10. The system of claim 9, wherein the laser assembly comprises a femto-second based laser beam.