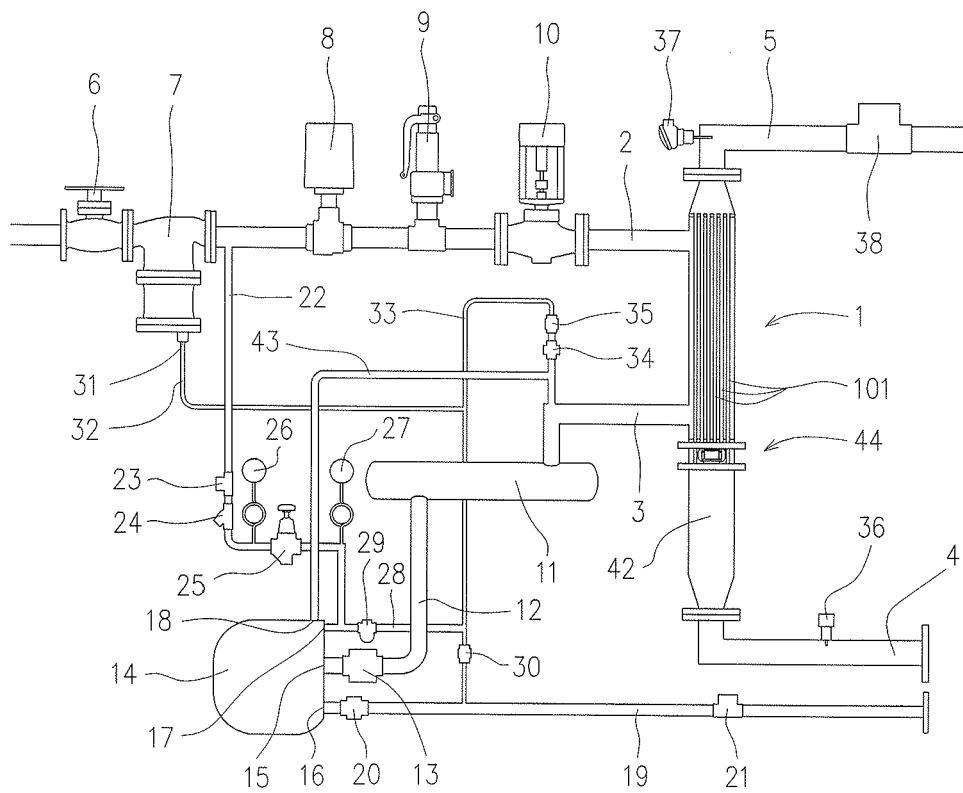
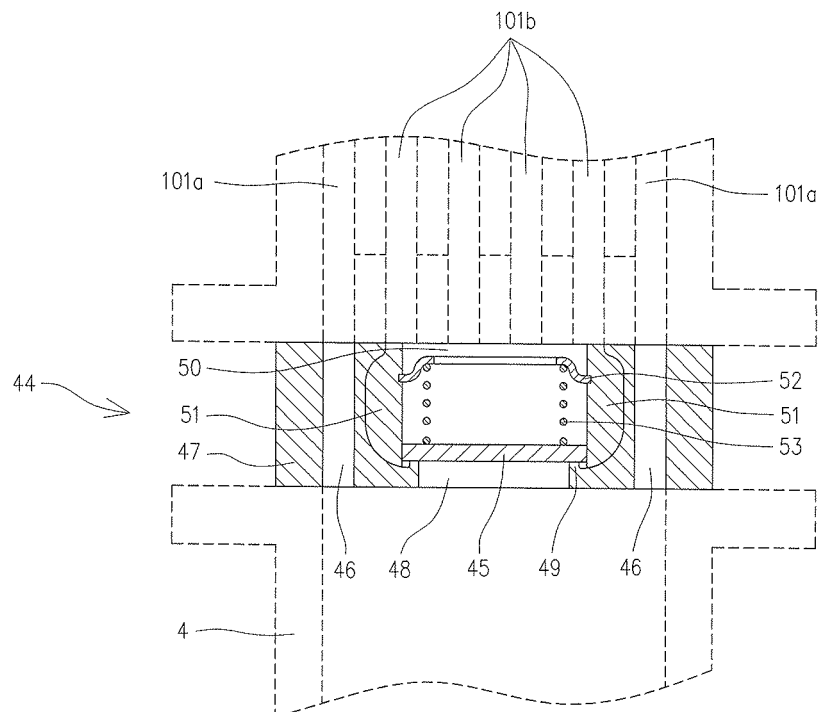


[図1]



[図2]



A cross-sectional view of a semiconductor device 64. The device features a central core 66 with a top layer 66a and a bottom layer 66b. The core is flanked by two side regions 67 and 68. A top layer 65 is positioned above the core, and a bottom layer 69 is positioned below it. The device is mounted on a substrate 70. A top layer 71 is positioned above the core, and a bottom layer 72 is positioned below it. A top layer 73 is positioned above the core, and a bottom layer 74 is positioned below it. A top layer 75 is positioned above the core, and a bottom layer 76 is positioned below it. A top layer 77 is positioned above the core, and a bottom layer 78 is positioned below it. A top layer 79 is positioned above the core, and a bottom layer 80 is positioned below it. A top layer 81 is positioned above the core, and a bottom layer 82 is positioned below it. A top layer 83 is positioned above the core, and a bottom layer 84 is positioned below it. A top layer 85 is positioned above the core, and a bottom layer 86 is positioned below it. A top layer 87 is positioned above the core, and a bottom layer 88 is positioned below it. A top layer 89 is positioned above the core, and a bottom layer 90 is positioned below it. A top layer 91 is positioned above the core, and a bottom layer 92 is positioned below it. A top layer 93 is positioned above the core, and a bottom layer 94 is positioned below it. A top layer 95 is positioned above the core, and a bottom layer 96 is positioned below it. A top layer 97 is positioned above the core, and a bottom layer 98 is positioned below it. A top layer 99 is positioned above the core, and a bottom layer 100 is positioned below it.

[図5]

