CLAIMS

We claim:

1. A phase change device (PCD) comprising:

a first semiconductor layer made of a first semiconductor material and having a first semiconductor thickness, the first semiconductor layer further having a first interface surface and a first electrode surface, the first interface surface and first electrode surface being on opposite sides of the first semiconductor layer, the first semiconductor material transitioning between a first amorphous state and a first crystalline state at one or more first conditions;

a second semiconductor layer made of a second semiconductor material and having a second semiconductor thickness, the second semiconductor layer further having a second interface surface and a second electrode surface, the second interface surface and second electrode surface being on opposite sides of the second semiconductor layer, the first interface surface and the second interface surface being in electrical, physical, and chemical contact with one another at an interface, and the second semiconductor material transitioning between a second amorphous state and a second crystalline state at one or more second conditions;

a first electrode in physical and electrical contact with the first electrode surface of the first semiconductor layer;

a second electrode in physical and electrical contact with the second electrode surface of the second semiconductor layer; and

a diffusion blocking layer at the interface between the first semiconductor layer and the second semiconductor layer,

wherein the first conditions and second conditions are different.

2. A PCD, as in Claim 1, where the first condition is a lower temperature and the second condition is a higher temperature.

3. A PCD, as in Claim 2, where the lower temperature and high temperatures are caused by a voltage pulse across the first electrode and the second electrode.

4. A PCD, as in Claim 3, where the voltage pulse is a reset pulse that has a voltage magnitude high enough to transition the first semiconductor material transitioning to the first amorphous state without transitioning the second semiconductor material from the second crystalline state.

5. A PCD, as in Claim 4, where the reset pulse has a reset pulse fall time fast enough so the first amorphous state does not transition to the first crystalline state.

6. A PCD, as in Claim 5, where the all the first semiconductor material is in the first amorphous state and a first resistance across the first semiconductor material in the first amorphous state is greater than the first resistance when part of the first semiconductor material is in the first crystalline state.

7. A PCD, as in Claim 6, where the voltage pulse is a set pulse that has a voltage magnitude high enough to transition the first semiconductor material transitioning out of the first amorphous state.

8. A PCD, as in Claim 7, where the set pulse has a gradual set pulse fall time slow enough so a first semiconductor crystalline layer epitaxially grows from the interface to split the first semiconductor layer into the first semiconductor crystalline layer with an epitaxial thickness less than the first semiconductor thickness and a first amorphous remainder layer with a remainder thickness.

9. A PCD, as in Claim 8, where the epitaxial thickness is determined by the set pulse fall time.

10. A PCD, as in Claim 1, where the first semiconductor layer is split into a first semiconductor crystalline layer with an epitaxial thickness less than the first semiconductor thickness and a first amorphous remainder layer with a remainder thickness, and where a first resistance across the first semiconductor material is less than the first resistance when the first semiconductor material is in the first amorphous state and greater than the first resistance when the first semiconductor material is in the first crystalline state.

11. A phase change device (PCD) comprising:

a first semiconductor layer made of a first semiconductor material and having a first semiconductor thickness, the first semiconductor layer further having a first interface surface and a first electrode surface, the first interface surface and first electrode surface being on opposite sides of the first semiconductor layer, the first semiconductor material split into a first semiconductor crystalline layer with an epitaxial thickness less than the first semiconductor thickness and a first amorphous remainder layer with a remainder thickness;

a second semiconductor layer made of a second semiconductor material and having a second semiconductor thickness, the second semiconductor layer further having a second interface surface and a second electrode surface, the second interface surface and second electrode surface being on opposite sides of the second semiconductor layer, the first interface surface and the second interface surface being in electrical, physical, and chemical contact with one another at an interface, and the second semiconductor material transitioning between a second amorphous state and a second crystalline state at one or more second conditions;

a first electrode in physical and electrical contact with the first electrode surface of the first semiconductor layer;

a second electrode in physical and electrical contact with the second electrode surface of the second semiconductor layer; and

a total resistance measured between the first electrode and second electrode.

12. A PCD, as in Claim 11, where the total resistance decreases as the epitaxial thickness increases.

13. A PCD, as in Claim 11, that can have a plurality of total resistance states by changing the epitaxial thickness.

14. A PCD, as in Claim 13, where one of the plurality of total resistance states is selected by a set voltage pulse.

15. A PCD, as in Claim 11, where the first semiconductor material is germanium and the second semiconductor material is silicon.

16. A PCD, as in claim 11, where the first semiconductor material is in a first crystalline state and the second semiconductor material is in a second crystalline state.

17. A PCD, as in claim 11, where the first semiconductor material is in a first amorphous state and the second semiconductor material is in a second crystalline state.

18. A PCD, as in claim 11, where the first semiconductor crystalline layer is in a crystalline state and the first amorphous remainder layer is in an amorphous state.

19. A PCD, as in claim 11, where the first semiconductor crystalline layer epitaxially grows from the interface.