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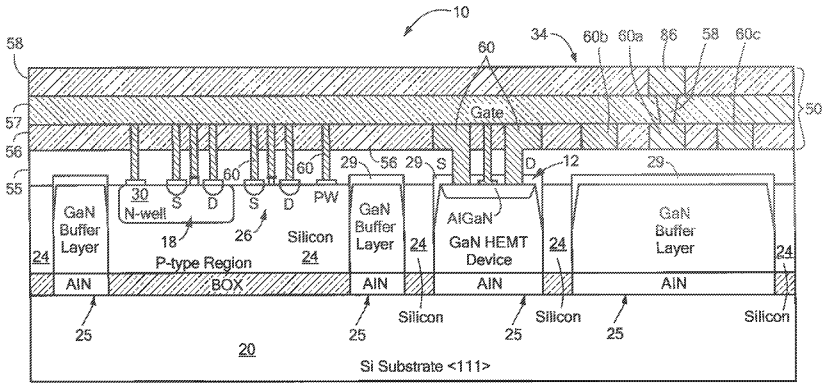


FIG. 5

(57) Abstract: A semiconductor structure provided having: a dielectric; a non-column III-V doped semiconductor layer disposed over the dielectric; and an isolation barrier comprising column III-V material disposed vertically through the semiconductor layer to the dielectric. In one embodiment, the semiconductor layer is silicon and has CMOS transistors disposed in the semiconductor layer above a first region of the dielectric and a III-V transistor disposed above a different region of the dielectric. The barrier electrically isolates the column III-V transistor from the CMOS transistors. In one embodiment, the structure includes a passive device disposed over the semiconductor layer and a plurality of laterally spaced III-V structures, the III-V structures being disposed under the passive device, the III-V structures passing vertically through the semiconductor layer to the insulating layer.

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