Description

This invention relates to image display systems and particularly to receivers or monitors of the type employing "progressive scanning" to reduce the visibility of vertical line structure of displayed images.

Progressive scan television receivers have been proposed wherein the horizontal scan rate is doubled and each line of video is displayed twice thereby providing a displayed image having twice the usual number of scan lines and thus reduced visibility of vertical line structure. In a typical progressive scan receiver each incoming horizontal line of video signal is stored in one of two memories. As one line is being stored in one memory, the line previously stored in the other memory is recovered or "read" twice thereby providing two lines of time compressed video within one standard line interval. The memory output is applied to a display having a doubled horizontal sweep rate synchronized with read-out of the memory thereby doubling the number of displayed lines of video signal.

An example of a progressive scan receiver in which the additional scan lines added to the display are obtained by interpolation from the original scan lines is described by K. H. Powers in U.S. Pat. US-A-4,400, 719 entitled TELEVISION DISPLAY SYSTEM WITH REDUCED LINE-SCAN ARTIFACTS which issued August 23, 1983. A receiver in which the added lines are replicas of the original lines is described by R.A. Dischert in U.S. Pat. US-A-4,415,931 entitled TELEVISION DISPLAY WITH DOUBLED HORIZONTAL LINES which issued November 15, 1983.

When implementing progressive scanning in a receiver with digital signal processing circuits, one may employ random access memories (RAM) for the line stores. Digital signal processing typically utilizes a coherent clock for purposes such as signal sampling (in the A/D converter), memory address control and other functions. For simplicity of chroma processing (e.g., decoding) it is advantageous to phase lock the clock to an integer multiple of the color subcarrier frequency. For NTSC standard video signals the memory write clock frequency is typically selected to be four-times that of the color subcarrier (4 Fsc) or about 14.3 MHz with a period of about 70 nanoseconds. One line of memory, for this clock frequency and the standard NTSC line period of about 63.5 microseconds, therefore requires 910 locations (addresses) in RAM to store 910 video samples or picture elements ("pixels" hereinafter). This memory requirement is invariant for NTSC standard signals because under the NTSC standard there are exactly 227.5 color subcarrier cycles per horizontal line. With D/A conversion done at four-times the color subcarrier frequency there are thus exactly 910 pixels per line (4 x 227.5). As long as the memory read clock is exactly double the frequency of the write clock, the result and "double-speed" or "time-compressed" pixels will have proper horizontal spacing and vertical alignment when displayed.

A problem exists in such progressive scan systems when processing for display what will be referred to hereinafter as "non-standard" video input signals. As used herein, the term non-standard refers to video input signals wherein the ratio of the color subcarrier frequency to the horizontal line frequency does not conform exactly to a specified broadcasting standard (e.g., 227.5 in the NTSC standard). Where, for example, the video source is a video disc player, a video casette recorder, a video game unit or some other non-standard source, the burst/line-frequency ratio may vary continuously within certain limits. These limits may include a significant variation from the standard ratio over a range of values. Under these conditions, the number of video samples (pixels) in a horizontal line period will not, in general, be an integer (e.g., 910). The number of 4 Fsc clock periods contained within one horizontal line period, in other words, may differ from the standard and this difference may include a fractional part of one clock cycle.

The deviation of the number of pixels per line from the standard value (e.g., 910) can result in a precession of the memory clock phase with respect to the incoming horizontal synchronizing signal phase. The effect of this precession or "phase-slip" or "skew" is that horizontal timing errors accumulate throughout each field scan interval. Moreover, the memory read clock precession relative to the double line-rate deflection will be twice as great as the precession of the memory write clock relative to the normal line-rate incoming video signal. This problem can cause accumulated horizontal timing errors which can result in full pixel discontinuities between occassional lines and other undesirable visible artifacts such as picture skew and ragged edges.

The need for skew correction of non-standard signals in a progressive scan processor employing a burst-locked clock has been recognized by Willis, et al. in U.S. Patent US-A-4593315 entitled PROGRESSIVE SCAN TELEVISION RECEIVER FOR NON-STANDARD SIGNALS issued June 3, 1986. In the Willis et al. system means are provided for measuring the phase of the speed-up memory read and write clocks with respect to the horizontal sweep of the display. Skew correction is provided from the speed-up memory as a function of the difference between the read and write clock skew measurements each time the memory is read.

In an exemplary embodiment of the Willis et al. system, clock skew measurements are made with respect to timing of the display sweep. It is recognized herein that under certain circumstances the sweep timing may vary, for example, when the overall brightness of a displayed scene suddenly changes. This, in turn, may alter the skew correction to the extent that visible artifacts may be produced from time to time. The present invention is directed in a first respect to reducing such undesirable artifacts.

The principles of the invention may be applied to a progressive scan display system including signal source means for supplying a video input signal of a given line rate, a write clock signal and a read clock signal to a video speed-up memory means which stores a horizontal line of the video input signal during a write cycle and recovers the stored line during each of first and second read cycles to provide a video output signal of double said given line rate to a display means synchronized therewith. The system further includes skew processing means comprising generator means for providing indicator signals related to skew of the read and write clock signals and skew corrector means responsive thereto for imparting an effective delay to the video output signal as a function of a difference between the read and write clock skew indicator during each memory read cycle.

In accordance with an aspect of the invention, the skew corrector means comprises first means for deriving both of the read and write clock skew indicator signals from the write clock signal and the video input signal and second means for doubling the values of the derived read clock skew indicator signal and for subtracting the write clock skew indicator signal thereform to form a control signal for controlling the effective delay of the video output signal during each ready cycle of the memory means.

In accordance with a further aspect of the invention the video output signal comprises a luminance component and a chrominance component and the skew corrector means includes means for effectively delaying the components as different functions of the delay control signal.

In accordance with a further feature of the invention the skew generator means includes means for measuring the horizontal line period of said video input signal and the skew corrector means includes means for initiating the second memory read cycle as a predetermined function of the line period measurement.

In the accompanying drawings:

FIGURE 1 is a block diagram of a television receiver embodying the invention;

FIGURE 2 is a timing diagram associated with the receiver of FIGURE 1;

FIGURE 3 is a block diagram of a progressive scan processor for use in the receiver of FIGURE 1;

FIGURE 4 is a block diagram of a horizontal processing unit for use in the receiver of FIGURE 1;

FIGURE 5 is a diagram associated with the processing unit of FIGURE 4; and

FIGURES 6 and 7 are block diagrams of delay devices suitable for use in the processor of FIGURE 3.

The receiver of FIGURE 1 includes an antenna (ANT.) input terminal 10 coupled via a tuner, IF amplifier and video detection unit 12 of conventional design to the input of an analog-to-digital converter 14. Unit 12 processes RF modulated video signals applied to terminal 10 to provide a baseband analog video signal S1 which is converted to digital form (signal S2) in (A/D) converter 14. The RF signal may be provided by an antenna, a tape recorder, video game, computer of other source. An auxilliary (AUX.) input terminal 16 is provided for obtaining the analog baseband video signal S1' from a source having provisions for baseband video output.

The digitized video signal S2 is applied to a video processing unit 18 of conventional design which provides various processing functions such as color separation, luminance peaking, contrast control, hue and saturation control, etc. The processed video signal S3 is applied to a burst locked clock 20, to a sync separator 22 and to a pair of progressive scan processors PSP-A and PSP-B (outlined in phantom). Clock 20 comprises a phase lock loop (PLL) keyed by horizontal sync pulses FH provided by sync separator 22 to provide read (FR) and write (FW) clock signals having frequencies locked to eight-times and four-times the frequency of the color subcarrier component (burst) of the video signal S3. For NTSC and PAL standard video input signals the 4 Fsc write clock frequencies are about 14,318 HMHz and 17,734 MHz, respectively. The read clock frequency (8Fsc) is double the write clock frequency.

The line rate of the video signal S3 is doubled by means of a pair of speed-up memories 40 and 42 in progressive scan processors PSP-A and PSP-B, respectively. Briefly, as one line of the video input signal is being stored in memory 40 in response to the 4 Fsc write clock FW, a line previously stored in memory 42 is recovered two times in response to the 8 Fsc read clock FR. The clock signals are then reversed and the next line of the video input signal is stored in memory 42 while memory 40 is being read twice. This read/write sequence is illustrated by diagrams G and H of FIGURE 2. The speeded-up video signals S4 and S5 provided by memories 40 and 42, respectively,

are applied to respective skew correctors 44 and 46 which remove clock skew errors as will be described to provide skew corrected double line rate output signals. Each skew corrector includes a respective output switch (e.g., a pair of tristate buffers, 95 and 97, shown in FIG. 3) synchronized with the memory read operations for coupling the output of corrector 44 to output bus 48 when memory 40 is being read and for coupling the output of corrector 46 to bus 48 when memory 42 is being read thereby producing the double line-rate video output signal S6 having the line sequence shown by sequence I of FIGURE 2.

The double line-rate video output signal S6 on bus 48 is converted to analog form via a digital-to-analog converter 26 and then to component form (R, G, B) by matrix unit 27 for application to a display 30 (e.g., a kinescope or projection device). The sweep of display 30 is synchronized with signal S6 by means of double line rate horizontal sync signals 2-FH provided by horizontal processing unit 32 and normal field rate vertical sync signal FV provided by vertical processing unit 34 whereby an image is produced on display 30 having double the usual number of horizontal lines and thus reduced visibility of line structure. An integrated circuit which provides the functions of sync separator 22, horizontal processing unit 32 and vertical processing unit 34 is the type DPU 2532 Deflection Processor Unit which is described at pages 47-72 of the databook "Digit 2000 NTSC Double-Scan VLSI Digital TV System" of ITT Intermetall, edition 1985/5. For completeness of explanation of the operation of the present invention, a detailed block diagram of unit 32 is included herein (FIG. 4) and discussed subsequently. The databook also includes a description at pages 41-46 of a type "PSP 2032 Progressive Scan Processor" integrated circuit which may be used for processor PSP-A and PSP-B. FIGURE 3 herein provides a detail block diagram of one of the two (identical) processors.

Without skew correction, the receiver of FIGURE 1 would be sensitive to skew errors because the read/write clock 20 is locked to burst. Thus, when non-standard input signals are received (as hereinbefore defined) the video input signal would be stored in the speed-up memory with one phase relative to the incoming sync and will be recovered from the memory and displayed with a diffferent phase relative to the display sync. If uncorrected, the skew errors will result in undesirable visual artifacts being displayed such as ragged vertical edges, pixel missalignment and whole pixel discontinuities during occasional lines.

Skew errors are corrected in the receiver of FIGURE 1 by means of correctors 44 and 46 which receive a skew data signal S7 in multiplexed form via conductor 33 from horizontal processing unit 32. The correction comprises delaying the video output signal of each speed-up memory in inverse proportion to the skew of the write clock and in direct proportion to the skew of the read clock. The term "skew" as used herein means the time difference, expressed in fractions of one clock cycle, of a given transition of a clock signal with respect to the horizontal synchronizing component of a video signal associated with the clock signal. The write clock skew is directly measured in unit 32 at the start of each memory write cycle and sent via conductor 33 to correctors 44 and 46 where it is used for two different purposes. Firstly, it is used to correct write skew errors of the speed-up memory which is writing (storing) a line of the video input signal. Secondly, it is used to correct read skew errors of the speed-up memory which is reading during the first read cycle of the memory. Recall that the read clock is operated at twice the frequency of the write clock. Accordingly, the read clock skew with respect to the double line-rate deflection has a predictable relationship with the write clock skew. Specifically, the read skew of each line recovered from speed-up memories at the start of a read cycle equals twice the value of the write skew measured at the start of the read cycle. This follows because the read clock period is exactly one half of the write clock period. Thus, a write skew error of a given value need only be doubled to represent a read skew error for correcting the video output signal during the first one of the two memory read cycles. Since the write skew data is used for two purposes, it is hereinafter referred to as the "primary" skew data.

Memories 40 and 42, it will be recalled, are read twice as quickly as they are written. If one were to use the measured write skew or "primary" skew for correcting all read skew errors, then each line read during the second memory read cycle would be displaced by one line's worth of skew that accumulated during the first read cycle thus producing a serrated edge effect in displayed images. This problem is solved by estimating the write clock skew with respect to the double line rate deflection and doubling the estimated value to arrive at the read clock skew for the lines produced during the second read cycle. The estimate of read clock skew for second memory read operations is performed by arithmetic circuits in processor 32 and is referred to herein as "secondary" skew. The calculation is made in unit 32 by measuring the period of the incoming horizontal sync pulses, dividing the period by two to give the period of the 2-FH deflection pulses and adding the result to the write clock skew. The fractional part of the sum represents the skew of the read clock with respect to the 2-FH deflection for all lines read from mem-

ory 50 during the second read cycle. This "secondary" skew data is stored alternately with the primary skew data in read skew latches in skew correctors 44 and 46 (as will be described) for controlling the delay of signal S6 directly in proportion to the read skew. Since the primary and secondary skew values are both derived from measurements of the write clock and not the read clock, these values of skew are doubled in correctors 44 and 46 when determining the delay imparted to the video output signal S6.

The primary and secondary skew data provided by processor 32 could be coupled directly to skew correctors 44 and 46. If done in parallel form a large number of conductors would be required. This problem is avoided by sending the primary and secondary skew data in time division multiplexed form to skew correctors 44 and 46 via a single conductor 33. The data format is illustrated in FIG. 2 by waveform D (not to scale). The primary skew data for lines N, N+1, etc. is identified by a low level of the signal waveform for two clock cycles. This identifying "preamble" is followed by a five bit word representing the primary skew data. Five bits provide a measurement resolution of one thirty-second of one clock cycle.

The timing for the primary skew data transmission is provided by leading edge of the write clock (up arrow, waveform C) which preceeds the center of the incoming sync pulses (waveform B) of each line of the video input signal (waveform A). The leading edge of the primary skew data (down arrow), in turn, is used in the progressive scan processors for producing a read/write (R/W) control signal (waveform E) for memories 40 and 42. This control signal is inverted for one of the memories whereby memories 40 and 42 read and write on alternate lines of the input signal as shown by waveforms G and H.

The secondary skew data is transmitted one half of one line period (T/2) of the video input signal after the primary skew data and is preceeded by a one clock period preamble to distinquish it from the primary skew data. As will be explained, the leading edge (down arrow) of the secondary skew data is used in the progressive scan processors for initiating the second memory read operations. To summarize briefly, the primary skew data is used for the three functions of: (1) correcting the write skew of the memory that is storing the video input signal; (2) correcting the read skew of the first read cycle of the memory that is reading a stored line and (3) controlling the read/write operations of the memories. The secondary skew data is used for the two functions of: (1) correcting the skew of the second read operation of the memory being received; and (2) initiating the start of the second memory read operation.

Waveforms E and F illustrate the memory control functions of the skew data for PSP-A. At the start of line N the "P" data (D) sets the read/write line low (E) and initiates a reset pulse (F) for memory 40. This starts a write operation which continues throughout line N. The "S" data is not used during writing by PSP-A and is simply ignored. At the start of line N+1 the P data places the read/write line high and resets the address counter of memory 40 thereby initiating the first memory read operation. One half line later (T/2) the "S" data is received and resets the address counter of memory 40 thereby initiating the second read operation. The operation of PSP-B is much the same except that the read/write signal is inverted so that PSP-A and PSP-B alternately read and write. In each the skew is used to initiate the second memory read operation by resetting the memory address counter.

The foregoing and further features of the invention are illustrated in greater detail in the block diagram of FIGURE 3 of PSP-A. The other speed up processor PSP-B is identical to PSP-A and is synchronized therewith by means of a master-slave control circuit to ensure that the read/write operations are complementary.

The serial skew data (S7 shown as D of FIG. 2) produced by horizontal processing unit 32 is supplied (via conductor 33) to input terminal 60 of PSP-A where it is converted to parallel form by means of a serial-in parallel-out (SIPO) register 62 for storage in a write skew latch 64 and a read skew latch 66 for correcting skew errors of the video output signal S4 of memory 40 as will be described. Signal S7 is also applied to a pulse detector 68 which detects the width of the preamble pulse and provides output pulses P and S identifying the data is being "primary" or "secondary" as previously discussed. The skew data identifying pulse P and S provide the dual functions of (1) controlling the timing of read/write operations of the speed-up memory 40 (outlined in phantom) and (2) determining which of the read and write latches 66 and 64 receives the skew data provided by SIPO register 62.

Memory timing operations are controlled by pulses P and S as follows. Pulse P is applied to a flip-flop 70 which toggles each time pulse P is detected thereby producing a read/write control signal (R/W) as shown by waveform E of FIGURE 2. Signal R/W is applied to a read/write control conductor 71 by means of an exclusive-OR gate 72 which, in combination with a tri-state buffer 73 forms a master/slave control circuit 74. Specifically, the output of flip-flop 70 is applied via buffer 73 to one input of gate 72 and via terminal 75 to a like terminal in PSP-B. A master slave selection terminal is coupled to the other input of gate 72 and to

the tristate control terminal of buffer 73. Terminal 76 selects which of the two processors, PSP-A or PSP-B, is the master and which is the slave to synchronize their respective memory read/write operations as follows. If terminal 76 is grounded, buffer 73 will be disabled. Terminal 75 then functions as an input for receiving R/W signals from PSP-B (the "master"). If, however, terminal 76 is connected to a source of positive voltage for PSP-A, then buffer 73 will be enabled and the R/W signal of flip flop 70 will be supplied to PSP-B and to gate 72 thus making PSP-A the "master" and PSP-B the "slave". The purpose of gate 72 is to ensure that the read/write signal for the master is complementary to that of the slave. This results because gate 72 inverts the R/W signal when terminal 76 is "high" (master operation) and does not invert signal R/W when terminal 76 is "low" (grounded).

The read/write signal on conductor 71 is combined with pulses P and S in a logic gate 78 to produce a reset pulse on conductor 77 for an address counter 56 in memory 40 in accordance with the following logic. Firstly, gate 78 couples pulse P to conductor 77 every time pulse P occurs. Secondly, gate 78 couples pulse S to reset conductor 77 whenever pulse S is present and the memory read/write line (71) is at a read state (low or high, depending on the logic convention used). In memory 40 conductor 71 is connected to the read/write control input of a random access memory (RAM) 50 and to a switch 57 which selectively applies the 4 Fsc write clock signal and the 8Fsc read clock signal to the clock input of address counter 56.

Memory 50 has inputs 52 and 54 for receiving luma (Y) and chroma (C) components of the video input signal S3 from video processor 18 and outputs for providing double line-rate luma (Y') and chroma (C') components of the video output signal S4. In operation signal R/W changes state and counter 56 is reset each time the primary skew data is received. In the write mode, switch 57 applies the 4 Fsc write clock signal to counter 56 thereby storing the video input signal in RAM 50 at the addresses indicated by counter 56. In this write mode, receipt of the secondary skew data has no effect on the memory operation as shown by waveforms D-G of FIGURE 2.

When the next primary skew data is received, pulse P toggles flip flop 70 and resets counter 56 via gate 78. This initiates the first read cycle of RAM 56 in which the signal previously stored in RAM 50 is recovered at the 8 Fsc read clock rate. It is instructive to note that if the video input signal S3 is a "standard" signal as hereinbefore defined, then it would occupy a total of 910 locations (addresses) in RAM 50 since there are exactly 910 pixels produced when an NTSC standard signal is clocked (sampled) at four-times the color subcarrier frequency (4 Fsc). Since, for such standard signals, the exact number of memory addresses is known, one could begin the second memory read cycle when 910 addresses had been read.

The timing of the start of the second memory read cycle, however, is not known beforehand where non-standard signals are involved. There may be more or less than 910 samples per line and the number may change significantly from line to line. The question, then, is when to start the second memory read operation for non-standard signals. The solution, for both standard and non-standard signals is to reset the address counter 56 whenever pulse S is received during a read operation. Recall that the secondary skew data is generated in processor 32 from a calculation of the half-period (T/2) of the video input signal S3 and is sent to PSP-A and PSP-B with this timing. Accordingly, if the period of the video input signal S3 varies, the start of the second memory read cycle will vary proportionally thereby automatically compensating for changes in the number of samples stored in RAM 50 for such non-standard signals.

The remaining elements of FIGURE 3 provide skew correction of signal S4 and output multiplexing as follows. The skew data provided by SIPO register 62 is stored in latches 64 and 66 by means of switches 80, 81 and 83 in response to signals P, R/W and S as follows. When primary skew data is received, switch 80 closes in response to pulse P. Concurrently, flip flop 70 toggles thereby changing the state of the read/write signal. If the change is from read-to-write, then switch 81 stores the primary skew data in the write latch 64 for correcting write clock skew errors of the line being stored in RAM 50. Conversely, if the change is from write-to-read, switch 81 will store the primary skew data in the read latch 66 for correcting read clock skew errors during the first memory read cycle. Switch 82 stores the secondary skew data in the read latch 66 when pulse S is detected for correcting read clock skew errors during the second memory read cycle. To summarize, latch 64 always contains the primary skew data at the start of each memory write cycle and latch 66 contains the primary skew data at the start of the first memory read cycle and the secondary skew data at the start of the second memory read cycle.

Since all skew data is measured using the write clock FW or calculated from write clock measurements, the read skew data in latch 66 is double by means of a multiplier 84 to express it in proportion to the period of the read clock as previously explained. The output of latch 64 is subtracted in subtractor 86 from the output of multiplier 84 to provide a difference signal S9 which varies directly

as the read skew and inversely as the write skew. Adder 88 adds a constant ("32") to signal S9 to avoid the need for "negative" delays when skew correcting the video output signal S4.

The skew correction signal S10 represents the net delay to be imparted to the double line-rate luminance Y' and chrominance C' components of signal S4 in terms of thirty-seconds of a clock period. This accuracy (5-bit resolution) is used in all arithmetic calculations to avoid an accumulation of arithmetic errors due, for example, to rounding-off or truncating numbers. It has been found that lower resolution may be used for the luma delay control signal (S11) and, additionally, that the chroma delay control signal (S12) may have substantially less resolution than that of the luma delay control signal if the value of the chroma control signal is "rounded-off" rather than being truncated. These functions are provided by divider 90 which divides signal S10 by two to develop the luma delay control signal S11. Divider 92 divides signal S10 by 32 to give chroma signal delays in terms of integer clock cycles. Adder 94 adds the number "16" to signal S10 prior to division by "32" to ensure that the result is rounded off to the nearest clock cycle rather than being truncated. As a result the chroma delay error relative to luma does not exceed more than one-half clock cycle even though the chroma is delayed in steps of one clock cycle by means of "coarse" delay unit 94. The term coarse delay, as used herein, means clock cycle delays.

For this purpose, unit 94 may comprise a conventional cascade connection of clocked latches and a selector switch responsive to signal S12 for selecting the output of the appropriate latch in proportion to the value of signal S12. Such an arrangement, as described, is shown in FIG. 7 herein where latches 702 and 704 act as a shift register and switch 706 selects taps in the register for delaying signal C' in one clock period steps.

The luma signal correction is provided by a cascade correction of coarse and fine delay units 96 and 98, respectively. The integer portion of signal S11 is applied to delay unit 96 for delaying luma signal Y' in integer clock cycle steps. The fine resolution fractional portion of signal S11 is applied to unit 98 for delaying signal Y' in steps of one-sixteenth of a clock cycle. For this purpose unit 98 might be implemented by means of a cascade connection of (unclocked) logic gates having delays of 1/16th clock cycle and a selector switch much as in FIGURE 7. Preferably, the delay provided by unit 98 is provided by means of an interpolator such as the two-point linear interpolator of FIGURE 6.

In FIGURE 6 the video signal to be delayed (Y') is applied via a multiplier 600 to one input of an adder 602 and via a cascade connection of another multiplier 604 and a delay latch 606 to the other input of adder 602. Latch 606 provides a one clock period delay (e.g., 35 nanoseconds). The multiplier coefficients (K and 1-K) are provided by a read only memory (ROM) 608 which varies the gain of multiplier 604 in direct proportion (K) to the skew data (S11) and varies the gain of multiplier 600 inversely (1-K) as the skew data whereby the ratio of delayed and non-delayed signals which are added in adder 602 are controlled by the values of the skew data. For example, when the skew data is zero the value of K is zero and the input signal passes without delay through multiplier 600 and adder 602 to the output. As K increases more of the delayed signal and less of the undelayed signal are added thereby increasing the delay of the output signal. In the limit (K=1) all of the input signal passes through the delay latch 606 to the output thereby delaying the signal by one full period of the clock.

FIGURE 4 is a detailed block diagram of horizontal processing unit 32. The principal elements, outlined in phantom, comprise: (1) a phase lock loop 402 which measures the primary skew and measures the period of the horizontal synchronizing component of the video input signal; (2) a skew and timing processor 404 which calculates the secondary skew from the primary skew and the period of the video input signal and multiplexes the skew (and timing) data to flicker reduction processors 44, 44; (3) a phase correction loop 406 which generates double line rate deflection pulses (2 FH) for display unit 30. An integrated circuit which includes these elements is type DPU 2532 Deflection Processor Unit which is described at pages 47-72 of the databook "Digit 2000 NTSC Double-Scan VLSI Digital TV System" of ITT Intermetall, edition 1985/5.

Phase lock loop 402 (outlined in phantom) includes a counter 410 which is clocked by the 4 Fsc write clock signal FW and rest by a comparator 412 when the count equals the period, T, of the horizontal synchronizing component, FH, of the video input signal S3. The period of signal S3 is determined by means of an accumulator 414 and an added 416 as follows. The sync signal FH from separator 22 is supplied through a low pass filter 418 to accumulator 414 which measures the time difference between the center of pulse FH and the occurrence of a master sync pulse MS provided by a decoder 420 coupled to the output of counter 410 (see FIG. 2, Waveform C). This time difference (or error) signal is scaled so as to represent the error in terms of cycles (and fractional cycles) of the write clock. It is then low pass filtered (in filter 419) and added in adder 416 to the number 910 which equals the number of 4 Fsc write clock periods in

one line of an NTSC standard signal. The period indicating signal, T, thus provided by adder 416 controls the threshold of comparator 412 thereby locking counter 410 to the horizontal synchronizing component of the video input signal.

When non-standard signals are received the period of counter 410 will be in error by an amount equal to the skew of the write clock signal. This results because counter 410 only counts integer cycles of the write clock signal whereas the period of the sync pulses FH may include a fraction of one clock cycle. Since the master sync pulse MS is generated by decoding the count of counter 410 it, too, will occur only at integer cycles of the write clock and so will also be in error by the amount of the write clock skew. The output of accumulator 414 will also include the skew error because it is synchronized by pulse MS. The remaining elements of PLL 402 provide the function of detecting the skew of the write clock and correcting the skew error of the period signal T.

Skew errors are detected by means of a latch 422 and an adder 424. Skew, it will be recalled, is the time difference between clock and sync expressed in fractions of a clock cycle as shown in FIG. 2. If it is assumed that the value of the period indicating signal, T, correctly represents the period of the video input signal, and if the fractional part of signal T is not zero then line-to-line changes in the skew will occur. As an example, if the period of signal FH is exactly 910.1 clock cycles long, then the write clock FW will precess with respect to sync (FH) at the rate of exactly 0.1 clock cycles per line. Thus, if the skew is zero at the start of line 1, it will be 0.1 at the start of line 2, 0.2 at the start of line 3 and so on. Skew data is generated by means of added 424 which adds the skew of the previous line (stored in latch 422) to the period signal T. The fractional part of the sum is then stored in latch 422 which thus functions as an accumulator for the skew data. The integer part of the sum is applied to comparator 412 for adjusting the period of counter 410.

Skew detection was based on the assumption that the period indicating signal T correctly represented the period of the video input signal. From the previous discussion, however, the accumulator 414 output contains the skew error because it is timed by pulse MS which can only occur at integer clock cycles. This error is removed from signal T by means of subtractor 426 which subtracts the detected skew data provided by latch 422 from the output of accumulator 414.

Accumulator 414 provides phase measurements to an accuracy finer than the resolution of the system clock (FW). It may be constructed as described, for example, in US pat. 4,471,299 which issued September 11, 1984. FIGURE 5 herein provides a simplified illustration of how the measurements may be made. Waveform A shows pulse FH as a function of time. Accumulator 414 essentially measures the areas of pulse FH which precede (Area 1) and follow (Area 2) pulse MS (Waveform B). This may be done by setting the accumulator count initially to zero, decrementing the count in proportion to the magnitude of pulse FH at each clock cycle (vertical tic marks) which preceed pulse MS and incrementing the count in proportion to the amplitude of pulse FH at each clock cycle after pulse MS. If pulse MS is exactly aligned with the center of pulse FH (as shown) then areas 1 and 2 will be equal and the accumulator output will be zero. If pulse MS precedes the center of pulse FH, then the areas will differ (as shown in by C and D) and the accumulator output will be proportional to the cross-hatched area (A2 - A1). This area represents the time difference between pulse MS and the true center of the horizontal sync pulse FH. One may then scale the accumulator output to express the result in terms of write clock cycles (and fractions thereof).

Skew and timing processor 404 includes arithmetic circuitry for deriving the secondary skew data from the primary skew data and multiplex circuitry for transmitting the skew data to PSP-A and PSP-B in the format shown by waveform D of FIGURE 2. The secondary skew data S is produced by an adder 430 which adds the primary or write clock skew data P provided by latch 422 to the output of a divider 432 which divides the period signal T by 2. The fractional part of the sum of the half period (T/2) signal and the write clock or primary skew P is the skew of the read clock (secondary skew, S) for the second memory read cycle.

The integer part of the sum signal provided by adder 430 is used to generate double line-rate (i.e., 2-H) timing pulses as follows. The ramp signal produced by counter 410 ranges from zero to some maximum value (e.g., 910 for NTSC standard signals or within a few counts of 910 for non-standard signals). A subtractor 434 subtracts the counter signal from a constant (labeled "delay control data") thereby producing an inverted ramp (as shown) which begins at a positive value determined by the value of the delay control signal and proceeds through zero to a negative peak. Zero crossings are easily detected in digital system and by varying the delay control signal, the zero crossing time of the ramp may be advanced or retarded. Line rate timing pulses (1-H) are produced by detecting zero of the ramp signal provided by subtractor 434. Double line rate (2H) timing pulses are produced by offsetting the ramp by one-half period (T/2) and detecting zero. (The offset is provided by adder 436, detection is provided by a

zero detector 442). By this means it is ensured that any change in the position of the line-rate (1-H) pulses will be tracked exactly by the double line-rate (2-H) pulses when the delay control signal is varied for such purposes, illustratively, as correcting the display sweep for processing delays the speeded-up video signal S4 may be subjected to.

The skew data is converted to serial form (FIG. 3 waveform D) by means of a parallel-in-serial-out (PISO) register 440 which is timed by pulses produced by zero detector 442. A line rate operated switch 444 alternatively applies the 1-H and 2-H ramp signals (from subtractor 434 and adder 436 respectively) to detector 442 and alternately supplies the primary (P) and secondary (S) skew data (from latch 422 and adder 430, respectively) to PISO 440. Detector 442 triggers PISO 440 to transmit the P or S skew data to PSP-A and PSP-B when the 1-H or 2-H ramp signal it receives equals zero. Switch 444 is controlled by a flip flop 446 which divides double line rate (2-H) deflection pulses produced in phase correction loop 406 by two. Thus, as shown in FIG. 2 by waveforms D, E and F, the primary and secondary skew signals are multiplexed to PSP-A and PSP-B and processed as previously described.

Phase correction loop 406 receives the ramp signal of subtractor 434 and the timing and skew signals from switch 444 and generates double line-rate deflection signals (2-FH) for display 30. The ramp output of subtractor 434 is detected by a decoder 450 to provide a delayed, line-rate (1-H) master sync pulse (MS'). The double line-rate sync pulses 2FH are produced by means of a phase detector 452 which compares the phase of flyback pulses FB produced by a reflection driver 454 (and digitized by a converter 456) with pulse MS'. Since the master MS' occurs on a clock edge, it contains skew errors which in will appear in the output of phase detector 452. These errors are removed by subtractor 453 which subtracts the skew data of processor 404 from the output of detector 452. The error signal (at the output of subtractor 453) produced by detector 452 is low pass filtered in filter 458, and added in adder 460 to the timing and skew signals provided by switch 444. The integer part of the resultant sum signal is zero detected by detector 462 thereby producing double line-rate pulses 2-FH which are applied to the deflection drive via a delay unit 464 controlled by the fractional part of the sum signal provided by adder 460 to thereby correct for clock skew errors in the deflection pulses (2-FH). In effect, the same primary and secondary skew signals used for correcting memory read/write operations are applied to the deflection driver to ensure that the display sweep is corrected in the same manner as the memory skew errors. Accordingly, skew errors which are corrected in the flicker reduction processor 24 are not re-introduced by deflection skew errors.

Claims

1. A progressive scan display system comprising:
   a) signal source means (18,20) for providing a video input signal (S3) of a given line rate, a read clock signal (FR), and a write clock signal (FW), said clock signals tending to exhibit skew when said video input signal is of non-standard form;
   b) video speed-up memory means (40,42) coupled to said signal source means and including means (50) for storing at least one line of said video input signal during a write cycle of said memory means and means (68,78,57) coupled thereto for performing first and second read cycles of said memory means in providing a video output signal of double said given line rate;
   c) display means (30) coupled to said memory means and synchronized therewith for displaying said video output signal; and
   d) skew corrector means (44,46) for generating read and write clock skew indicator signals and for imparting an effective delay to said video output signal as a direct function of said read clock skew indicator signal and as an inverse function of said write clock skew indicator signal during each said read cycle of said memory means for reducing visible artifacts on said display means due to skew of said clock signals;
   characterised in that said skew corrector means comprises:
   e) first means (32) coupled to said signal source means for deriving said read and write clock skew indicator signals from said write clock signal and said video input signal; and
   f) second means (84,86) in said skew corrector means for doubling the value of the derived read clock skew indicating signal for each said read cycle of said memory means and for subtracting therefrom the value of said write clock skew indicating signal of the preceeding write cycle of said memory means to form a control signal (59) for controlling the effective delay (94;96,98) imparted to said video output signal.

2. A system as recited in Claim 1 further comprising third means (68,FF,72) in said skew corrector means responsive to said clock skew indicator signals for initiating (R/W) said read and write cycles of said memory means.

zero detector 442). By this means it is ensured that any change in the position of the line-rate (1-H) pulses will be tracked exactly by the double line-rate (2-H) pulses when the delay control signal is varied for such purposes, illustratively, as correcting the display sweep for processing delays the speeded-up video signal S4 may be subjected to.

The skew data is converted to serial form (FIG. 3 waveform D) by means of a parallel-in-serial-out (PISO) register 440 which is timed by pulses produced by zero detector 442. A line rate operated switch 444 alternatively applies the 1-H and 2-H ramp signals (from subtractor 434 and adder 436 respectively) to detector 442 and alternately supplies the primary (P) and secondary (S) skew data (from latch 422 and adder 430, respectively) to PISO 440. Detector 442 triggers PISO 440 to transmit the P or S skew data to PSP-A and PSP-B when the 1-H or 2-H ramp signal it receives equals zero. Switch 444 is controlled by a flip flop 446 which divides double line rate (2-H) deflection pulses produced in phase correction loop 406 by two. Thus, as shown in FIG. 2 by waveforms D, E and F, the primary and secondary skew signals are multiplexed to PSP-A and PSP-B and processed as previously described.

Phase correction loop 406 receives the ramp signal of subtractor 434 and the timing and skew signals from switch 444 and generates double line-rate deflection signals (2-FH) for display 30. The ramp output of subtractor 434 is detected by a decoder 450 to provide a delayed, line-rate (1-H) master sync pulse (MS'). The double line-rate sync pulses 2FH are produced by means of a phase detector 452 which compares the phase of flyback pulses FB produced by a reflection driver 454 (and digitized by a converter 456) with pulse MS'. Since the master MS' occurs on a clock edge, it contains skew errors which in will appear in the output of phase detector 452. These errors are removed by subtractor 453 which subtracts the skew data of processor 404 from the output of detector 452. The error signal (at the output of subtractor 453) produced by detector 452 is low pass filtered in filter 458, and added in adder 460 to the timing and skew signals provided by switch 444. The integer part of the resultant sum signal is zero detected by detector 462 thereby producing double line-rate pulses 2-FH which are applied to the deflection drive via a delay unit 464 controlled by the fractional part of the sum signal provided by adder 460 to thereby correct for clock skew errors in the deflection pulses (2-FH). In effect, the same primary and secondary skew signals used for correcting memory read/write operations are applied to the deflection driver to ensure that the display sweep is corrected in the same manner as the memory skew errors. Accordingly, skew errors which are corrected in the flicker reduction processor 24 are not re-introduced by deflection skew errors.

Claims

1. A progressive scan display system comprising:
   a) signal source means (18,20) for providing a video input signal (S3) of a given line rate, a read clock signal (FR), and a write clock signal (FW), said clock signals tending to exhibit skew when said video input signal is of non-standard form;
   b) video speed-up memory means (40,42) coupled to said signal source means and including means (50) for storing at least one line of said video input signal during a write cycle of said memory means and means (68,78,57) coupled thereto for performing first and second read cycles of said memory means in providing a video output signal of double said given line rate;
   c) display means (30) coupled to said memory means and synchronized therewith for displaying said video output signal; and
   d) skew corrector means (44,46) for generating read and write clock skew indicator signals and for imparting an effective delay to said video output signal as a direct function of said read clock skew indicator signal and as an inverse function of said write clock skew indicator signal during each said read cycle of said memory means for reducing visible artifacts on said display means due to skew of said clock signals;
   characterised in that said skew corrector means comprises:
   e) first means (32) coupled to said signal source means for deriving said read and write clock skew indicator signals from said write clock signal and said video input signal; and
   f) second means (84,86) in said skew corrector means for doubling the value of the derived read clock skew indicating signal for each said read cycle of said memory means and for subtracting therefrom the value of said write clock skew indicating signal of the preceeding write cycle of said memory means to form a control signal (59) for controlling the effective delay (94;96,98) imparted to said video output signal.

2. A system as recited in Claim 1 further comprising third means (68,FF,72) in said skew corrector means responsive to said clock skew indicator signals for initiating (R/W) said read and write cycles of said memory means.

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3. A system as recited in Claim 1 wherein said video output signal comprises a luminance (Y') and a chrominance (c') component and wherein said second means includes means (96,98,94) for effectively delaying said components as different functions of said control signal.

4. A system as recited in Claim 1 wherein:

said first means comprises measurement means (404) for providing a primary skew indicating signal (P) representative of skew of said write clock signal at the beginning of each write cycle and each first read cycle of said memory means, and a secondary skew indicating signal (S) representative of skew of said write clock at the beginning of said second memory read cycle; and

said second means comprises a first storage means (64) for storing said primary skew indicating signal at the beginning of said write cycle and a second storage means (66) for alternately storing said primary and secondary skew indicating signals at the beginning of said first and second read cycles, respectively, and means (84,86) coupled to said storage means for forming said delay control signal.

5. A system as recited in Claim 4 further comprising third means (68,78,FF,72) responsive to said primary and secondary skew indicating signals for initiating read and write cycles of said memory means.

6. A system as recited in Claim 1 wherein said first means includes means (430) for adding to said write clock skew indicating signal (from 422) a signal (T2) representing a half-line period of said video input signal, to form a sum signal having integer and fraction parts, and means (436,442) responsive to an integer part of said sum signal for producing a control pulse, said second means including means (68,78) responsive to said control pulse for initiating said second memory read cycle.

7. A system as recited in Claim 1 wherein said video output signal comprises a luminance component (Y') and a chrominance (C') component, said delay control signal (S9) comprises a binary signal manifestation, and said second means includes arithmetic means (88,94,92) for rounding off fractional portions of said binary signal manifestation to provide a modified signal manifestation for controlling the effective delay (94) imparted to said chrominance component.

8. A progressive scan display system comprising a video speed-up memory means (40,42) for doubling the horizontal line rate of a video input signal supplied thereto to provide a double line-rate video output signal (S4,S5) to a display means (30), a source (20) of read and write clock signals (FR,FW) coupled to said memory means for controlling read and write operations thereof, and skew correction means (44,46) for imparting variable delay to said double line-rate video output signal for reducing visible artifacts on said display means caused by skew of said clock signals, characterised in that said skew correction means comprises:

first means (402) responsive to said video input signal and said write clock signal for providing a write clock skew indicating signal ('PRIMARY SKEW');

second means (430-436) coupled to the first means for deriving a read clock skew indicating signal from said write clock skew indicating signal; and

third means (94;96,98) coupled to said memory means for delaying said video output signal as a function of a difference (86) between said write clock skew indicating signal and a multiple (84) of said read clock skew indicating signal to minimize said visible artifacts on said display means.

9. A display system as recited in Claim 8 wherein said third means includes means (84) for doubling said read clock skew indicating signal and means (86) for subtracting therefrom said write clock skew indicating signal to form a delay control signal, said delay means being responsive thereto for delaying said video output signal.

10. A display system as recited in Claim 8 wherein said video output signal comprises a luminance component (Y') and a chrominance component (C') and said delay means is responsive to said delay control signal for imparting higher resolution delays to said luminance component (96,98) than to said chrominance component (94).

11. A display system as recited in Claim 8 wherein said second means includes means (430) for adding to said write clock skew indicating signal a signal representing a half-line period of said video input signal, to form a sum signal having integer and fractional parts, said fractional part of said sum signal corresponding to said read clock skew indicating signal for each second read cycle of said memory means.

12. A display system as recited in Claim 8 wherein said video speed-up memory means is of a type in which each write cycle thereof is followed by first and second read cycles and wherein said third means includes a first memory (64) for storing said write skew indicating signal at the start of each said write cycle and a second memory (66) for alternately storing said write skew and said read skew indicating signals at the start of respective ones of said first and second read cycles.

Revendications

1. Un système d'affichage non-entrelacé comprenant :
   a) un moyen source de signaux (18,20) pour produire un signal d'entrée vidéo (S3) d' une fréquence de ligne donnée, un signal d'horloge de lecture (FR) et un signal d'horloge d'écriture (FW), lesdits signaux d'horloge tendant à présenter un désalignement lorsque le signal d'entrée vidéo est d'un format hors norme ;
   b) un moyen mémoire d'accélération vidéo (40,42) couplé audit moyen source des signaux et comprenant un moyen (50) pour stocker au moins une ligne dudit signal d'entrée vidéo pendant un cycle d'écriture dudit moyen mémoire et un moyen (68,78,57) couplé à celui-ci pour accomplir des premier,et second cycles de lecture dudit moyen mémoire en produisant un signal de sortie vidéo du double de la fréquence de ligne donnée ;
   c) un moyen d'affichage (30) couplé audit moyen mémoire et synchronisé avec celui-ci pour afficher le signal de sortie vidéo ;
   d) un moyen correcteur de désalignement (44,46) pour produire des signaux d'indication de désalignement d'horloge de lecture et d'écriture et pour impartir un retard effectif audit signal de sortie vidéo en une fonction directe dudit signal d'indication de désalignement d'horloge de lecture et en une fonction inverse dudit signal d'indication de désalignement d'horloge d'écriture pendant chaque cycle de lecture dudit moyen mémoire pour réduire des artéfacts visibles au moyen d'affichage dûs au désalignement des signaux d'horloge ;
   caractérisé en ce que le moyen correcteur de désalignement comprend :
   e) un premier moyen (32) couplé au moyen source de signaux pour dériver lesdits signaux d'indication de désalignement d'horloge de lecture et d'écriture du signal d'horloge d'écriture et du signal d'entrée vidéo et,
   f) un second moyen (84,86) dans le moyen correcteur de désalignement pour doubler la valeur du signal d'indication de désalignement d'horloge de lecture dérivée pendant chaque cycle de lecture du moyen mémoire et pour soustraire de celui-ci la valeur du signal d'indication de désalignement d'horloge d'écriture du cycle d'écriture précédent du moyen mémoire pour former un signal de commande (59) commandant le retard effectif (94 ; 96 ; 98) imparti audit signal de sortie vidéo.

2. Un système selon la revendication 1 comprenant de plus un troisième moyen (68, FF,72) dans le moyen correcteur de désalignement précité répondant aux signaux d'indication de désalignement d'horloge précités pour initialiser (R/W) les cycles de lecture et d'écriture précités du moyen mémoire précité.

3. Un système selon la revendication 1 où le signal de sortie vidéo précité comprend une composante de luminance (Y') et de chrominance (C') et où le second moyen précité comprend un moyen (96,98,94) pour retarder effectivement lesdites composantes comme des fonctions différentes du signal de commande précité.

4. Un système selon la revendication 1 où :

   le premier moyen précité comprend un moyen de mesure (404) pour produire un signal primaire d'indication de désalignement (P) représentatif du désalignement du signal d'horloge d'écriture précité au début de chaque cycle d'écriture et de chaque premier cycle de lecture du moyen mémoire, et un signal secondaire d'indication de désalignement (S) représentatif du désalignement dudit signal d'horloge d'écriture au début du second cycle de lecture de la mémoire ; et

   le second moyen précité comprend un premier moyen de stockage (64) pour stocker le signal primaire d'indication de désalignement au début ducycle d'écriure et un second moyen de stockage (66) pour stocker alternativement les signaux primaire et secondaire d'indication de désalignement au début respectivement des premier et second cycles de lecture, et un moyen (84,86) couplé au moyen de stockage pour former le signal de commande de retard précité.

5. Un système selon la revendication 4 compre-

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nant de plus un troisième moyen (68,78,FF,72) répondant aux signaux primaire et secondaire d'indication de désalignement pour initialiser les cycles de lecture et d'écriture du moyen mémoire précité.

6. Un système selon la revendication 1 où le premier moyen précité comprend un moyen (430) pour additionner au signal d'indication de désalignement d'horloge d'écriture (de 422) un signal (T2) représentant une période de moitié de ligne du signal d'entrée vidéo précité pour former un signal de somme ayant des parties entière et fractionnelle, et un moyen (436,442) répondant à une partie entière du signal de somme pour produire une impulsion de commande, le second moyen précité comprenant un moyen (68,78) répondant à l'impulsion de commande pour initialiser le second cycle de lecture de la mémoire.

7. Un système selon la revendication 1 où le signal de sortie de vidéo précité comprend un composante de luminance (Y') et une composante de chrominance (C'), le signal de commande de retard précité (S9) comprend une représentation d'un signal binaire, et le second moyen précité comprend un moyen arithémique (88,94,92) pour arrondir les parties fractionnelles de la représentation du signal binaire pour produire une représentation modifiée du signal pour commander le retard effectif (94) imparti à la composante de chrominance.

8. Un système d'affichage entrelacé comprenand un moyen mémoire d'accélération vidéo (40,42) pour doubler la fréquence de ligne horizontale d'un signal d'entrée vidéo appliqué à celui-ci pour produire un signal de sortie vidéo de fréquence de ligne double (S4,S5) à un moyen d'affichage (30),une source (20) de signaux d'horloge de lecture et d'écriture (FR,Fw) couplée au moyen mémoire pour commander les fonctionnements de lecture et d'écriture de celui-ci, et un moyen de correction de désalignement (44,46) pour impartir un retard variable au signal de sortie vidéo de fréquence de ligne double pour réduire des artéfacts visibles au moyen d'affichage provoqués par le désalignement desdits signaux d'horloge, caractérisé en ce que le moyen de correction de désalignement comprend :

un premier moyen (402) répondant au signal d'entrée vidéo et au signal d'horloge d'écriture pour produire un signal d'indication de déplacement d'horloge d'écriture (DESALIGNEMENT PRIMAIRE) ;

un second moyen (430 - 436) couplé au premier moyen pour dériver un signal d'indication de désalignement d'horloge de lecture du signal d'indication de désalignement d'horloge d'écriture ; et

un troisième moyen (94,96,98) couplé au moyen mémoire pour retarder le signal de sortie vidéo comme une fonction d'une différence (86) entre le signal d'indication de désalignement d'horloge d'écriture et un multiple (84) du signal d'indication de désalignement d'horloge de lecture pour minimiser les artéfacts visibles précités au moyen d'affichage précité.

9. Un système d'affichage selon la revendication 8 où le troisième moyen précité comprend un moyen (84) pour doubler le signal d'indication de désalignement d'horloge de lecture et un moyen (86) pour soustraire de celui-ci le signal d'indication de désalignement d'horloge d'écriture pour former un signal de commande de retard, ledit moyen à retard répondant à celui-ci pour retarder le signal de sortie vidéo.

10. Un système d'affichage selon la revendication 8 où le signal de sortie vidéo précité comprend une composante de luminance (Y') et une composante de chrominance (C') et le moyen à retard précité répond audit signal de retard pour impartir des retards de résolution plus élevée à la composante de luminance (96,98) qu'à la composante de chrominance (94).

11. Un système d'affichage selon la revendication 8 où le second moyen précité comprend un moyen (430) pour additionner au signal d'indication de désalignement d'horloge d'écriture précité un signal représentant une période de moitié de ligne du signal d'entrée vidéo précité pour former un signal de somme ayant des partiesentière et fractionnelle, la partie fractionnelle du signal de somme correspondant au signal d'indication de désalignement d'horloge de lecture pendant chaque second cycle de lecture du moyen mémoire précité.

12. Un système d'affichage selon la revendication 8 où le moyen mémoire d'accélération vidéo est d'un type dans lequel chaque cycle d'écriture de celui-ci est suivi de premier et second cycles de lecture et où le troisième moyen précité comprend une première mémoire (64) pour stocker le signal d'indication de désalignement d'écriture précité au départ de cha-

que cycle d'écriture précité et une seconde mémoire (66) pour stocker alternativement les signaux d'indication de désalignement d'écriture et de lecture au départ des cycles respectifs des premier et second cycles de lecture.

Patentansprüche

1. Anzeigesystem mit progressiver Abtastung, mit
   a) einer Signalquelle (18,20) zur Lieferung eines Videoeingangssignals (53) einer gegebenen Zeilenfrequenz, eines Lesetaktsignals (FR) und eines Schreibtaktsignals (FW), wobei diese Taktsignale bei nicht normgerechten Eingangssignalen zu Verschiebungen neigen,
   b) eine mit der Signalquelle gekoppelte Videobeschleunigungsspeichereinrichtung (40,42), die einen Speicher (50) zur Speicherung mindestens einer Zeile des Videoeingangssignals während eines Schreibzyklus der Speicheranordnung und eine mit dieser gekoppelte Einrichtung (68,78,57) zur Durchführung erster und Zweiter Lesezyklen der Speicheranordnung im Sinne einer Lieferung eines Videoausgangssignals, dessen Zeilenfrequenz doppelt so groß wie die gegebene Zeilenfrequenz ist, enthält,
   c) eine mit der Speicheranordnung gekoppelte und mit dieser synchronisierte Darstellungseinrichtung (30) zur Wiedergabe des Videoausgangssignals und
   d) einer verschiebungskorrektureinrichtung (44,46), welche Lese- und Schreibtaktverschiebungsindikatorsignale erzeugt und das Videoausgangssignal effektiv verzögert in direkter Abhängigkeit von den Lesetaktverschiebungsindikatorsignalen und in umgekehrter Abhängigkeit von den Schbreibtaktverschiebungsindikatorsignalen während jedes Lesezyklus der Speicheranordnung zur Reduzierung sichtbarer Fehler auf der Darstellungseinrichtung infolge von Verschiebungen der Taktsignale,
   dadurch gekennzeichnet, daß die Korrektureinrichtung umfaßt:
   e) eine mit der Signalquelle gekoppelte erste Einrichtung (32) zur Ableitung der Lese- und Schreibtaktverschiebungsindikatorsignale von dem Schreibtaktsignal und dem Videoeingangssignal und
   f) eine in der verschiebungskorrektureinrichtung vorgesehene zweite Einrichtung (84,86), welche den Wert des abgeleiteten Lesetaktverschiebungsindikatorsignals für jeden der Lesezyklen der Speicheranordnung verdoppelt und davon den Wert des Schreibtaktverschiebungsindikatorsignals des vorangehenden Schreibzyklus der Speicheranordnung subtrahiert zur Bildung eines Regelsignals (59) zur Regelung der effektiven Verzögerung (94;96,98), die dem Videoausgangssignal erteilt wird.

2. System nach Anspruch 1, gekennzeichnet durch eine in der Verschiebungskorrektureinrichtung vorgesehene dritte Einrichtung (68,FF,72), welche in Abhängigkeit von den Taktverschiebungsindikatorsignalen die Lese- und Schreibzyklen der Speicheranordnung einleitet (R/W).

3. System nach Anspruch 1, dadurch gekennzeichnet, daß das Videoausgangssignal eine Leuchtdichtekomponente (Y') und eine Farbkomponente (C') enthält und daß die zweite Einrichtung eine Verzögerungseinrichtung (96,98,94) zur effektiven Verzögerung der Komponenten in unterschiedlicher Abhängigkeit von dem Regelsignal enthält.

4. System nach Anspruch 1, dadurch gekennzeichnet, daß die erste Einrichtung eine Meßeinrichtung (404) zur Lieferung eines Primärverschiebungsindikatorsignals (P) als Maß für die Verschiebung des Schreibtaktsignals zu Beginn jedes Schreibzyklus und jedes ersten Zyklus der Speicheranordnung und eines Sekundärverschiebungsindikatorsignals (S) als Maß für die Verschiebung des Schreibtaktes zu Beginn des zweiten Speicherauslesezyklus enthält, und daß die zweite Einrichtung einen ersten Speicher (64) zur Speicherung des Primärverschiebungsindikatorsignals zu Beginn des Schreibzyklus und einen zweiten Speicher (66) zur abwechselnden Speicherung der Primär- und Sekundärverschiebungsindikatorsignalezu Beginn der ersten bzw. zweiten Lesezyklen sowie eine mit den Speichern gekoppelte Einrichtung (84,86) zur Bildung des Verzögerungsregelsignals enthält.

5. System nach Anspruch 4, gekennzeichnet durch eine dritte Einrichtung (68,78,FF,72), welche unter Steuerung durch die Primär- und Sekundärverschiebungsindikatorsignale die Lese- und Schreibzyklen der Speicher einleitet.

6. System nach Anspruch 1, dadurch gekennzeichnet, daß die erste Einrichtung einen Addierer (430) zur Addition des Schreibtaktverschiebungsindikatorsignals (von 422) mit einem eine Halbzeilenperiode des Videoeingangssignals darstellenden Signal (T2) zur Bildung eines Summensignals mit ganzzahligen Anteilen und Bruchteilen, und eine Einrichtung

(436,442) enthält, die unter Steuerung durch einen ganzzahligen Anteil des Summensignals einen Regelimpuls erzeugt, und daß die zweite Einrichtung eine durch den Regelimpuls gesteuerte Einrichtung (68,78) zur Einleitung des zweiten Speicherlesezyklus enthält.

7. System nach Anspruch 1, dadurch gekennzeichnet, daß das Videoausgangssignal eine Leuchtdichtekomponente (y') und eine Farbkomponente (C') enthält, daß das Verzögerungsregelsignal (S9) eine Binärsignaldarstellung aufweist und daß die zweite Einrichtung eine Arithmetikschaltung (88,94,92) zur Rundung von Bruchteilen der Binärsignaldarstellung zur Lieferung einer modifizierten Signaldarstellung zur Regelung der effektiven Verzögerung (94) enthält, welche der Farbkomponente erteilt wird.

8. Sichtgerätsystem mit progressiver Abtastung mit einer Videobeschleunigungsspeicheranordnung (40,42) zur Verdoppelung der Horizontalzeilenfrequenz eines zugeführten Videoeingangssignals zur Lieferung eines Videoausgangssignals (S4,S5)der doppelten Zeilenfrequenz an ein Sichtgerät (30), mit einer Lese- und Schreibtaktsignalquelle (20,FR,FW), die mit der Speicheranordnung zur Steuerung von deren Lese- und Schreibvorgängen gekoppelt ist, mit einer Verschiebungskorrektureinrichtung (44,46), welche dem Videoausgangssignal der doppelten Zeilenfrequenz eine variable Verzögerung erteilt zur Reduzierung sichtbarer Bildfehler auf dem Sichtgerät infolge Verschiebungen der Taktsignale, **dadurch gekennzeichnet,** daß die Verschiebungskorrektureinrichtung aufweist:

eine erste Einrichtung (402), die unter Steuerung durch das Videoeingangssignal und das Schreibtaktsignal ein Schreibtaktverschiebungsindikatorsignal (Primärverschiebungsignal) liefert,

eine mit der ersten Einrichtung gekoppelte zweite Einrichtung (430,436) zur Ableitung eines Lesetaktverschiebungsindikatorsignals aus dem Schreibtaktverschiebungsindikatorsignals und

eine mit der Speicheranordnung gekoppelte dritte Einrichtung (94,96,98) zur Verzögerung des Videoausgangssignals in Abhängigkeit von einer Differenz (86) zwischen dem Schreibtaktverschiebungsindikatorsignal und einem Vielfachen (84) des Lesetaktverschiebungsindikatorsignals im Sinne einer Minimalisierung sichtbarer Bildfehler auf dem Sichtgerät.

9. System nach Anspruch 8, dadurch gekennzeichnet, daß die dritte Einrichtung eine Verdoppelungseinrichtung (84) zur Verdoppelung des Lesetaktverschiebungsindikatorsignals und einen Subtrahierer (86), welcher davon das Schreibtaktverschiebungsindikatorsignal subtrahiert zur Bildung eines Verzögerungsregelsignals, und eine Verzögerungseinrichtung enthält, die in Abhängigkeit von dem Verzögerungsregelsignal das Videoausgangssignal verzögert.

10. System nach Anspruch 8, dadurch gekennzeichnet, daß das Videoausgangssignal eine Leuchtdichtekomponente (y') und eine Farbkomponente (C') enthält, und daß die Verzögerungseinrichtung in Abhängigkeit von dem Verzögerungsregelsignal der Leuchtdichtekomponente (96,98) Verzögerungen mit höherer Auflösung als der Farbkomponente (94) erteilt.

11. System nach Anspruch 8, dadurch gekennzeichnet, daß die zweite Einrichtung einen Addierer (430) zur Addition des Schreibtaktverschiebungsindikatorsignals mit einem eine Halbzeilenperiode des Videoeingangssignals darstellenden Signal zur Bildung eines Summensignals enthält, das ganzzahlige Anteile und Bruchteile hat, wobei der ganzzahlige Anteil des Summensignals dem Lesetaktverschiebungsindikatorsignal für jeden zweiten Lesezyklus der Speicheranordnung entspricht.

12. System nach Anspruch 8, dadurch gekennzeichnet, daß die Videobeschleunigungsspeicheranordnung von einem Typ ist, bei dem jedem Schreibzyklus ein erster und ein zweiter Lesezyklus folgt, und daß die dritte Einrichtung einen ersten Speicher (64) zur Speicherung des Schreibverschiebungsindikatorsignals, zu Beginn jedes der Schreibzyklen und einen zweiten Speicher (66) zur abwechselnden Speicherung der Schreib- und der Leseverschiebungsindikatorsignale zu Beginn entsprechender der ersten und zweiten Lesezyklen enthält.