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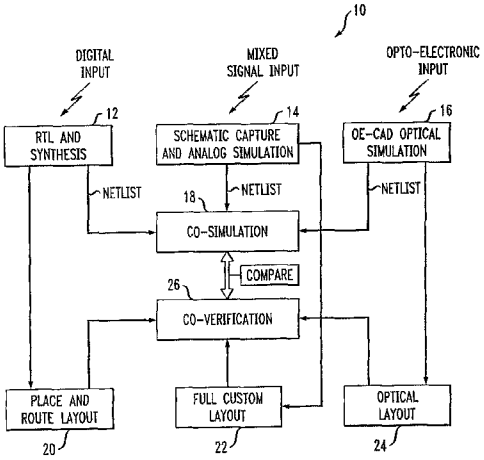
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(54) **Title:** INTEGRATED APPROACH FOR DESIGN, SIMULATION AND VERIFICATION OF MONOLITHIC, SILICON-BASED OPTO-ELECTRONIC CIRCUITS



(57) **Abstract:** Computer-aided design (CAD) tools are used to perform the integrated design, verification and layout of electrical and optical components in a monolithic, silicon-based electro-optic chip. Separate top-level behavioral logic designs are prepared for the three different types of elements included within the final, silicon-based monolithic structure: (1) digital electronic integrated circuit elements; (2) analog/mixed signal electronic integrated circuit elements; and (3) opto-electronic elements (including passive and active optical elements). Once the behavioral logic design is completed, the results are combined and co-simulated. A physical layout design is developed and verified for each different type of element in the circuit. The separate physical layouts are then co-verified, to assess the properties of the overall physical design. The results of the co-simulation are compared to the results of the co-verification, with alterations made in the logic design and/or the physical layout until the desired operating parameters are obtained. Once the desired results are generated, conventional wafer-level fabrication operations are then considered to provide a final product ("tape out").

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