

ABSTRACT

Embodiments of the present disclosure provide a chip stack package including a first semiconductor chip having a front bump on a
5 first surface, a second semiconductor chip stacked on a second surface
of the first semiconductor chip opposite the first surface, a carrier bump
bonded to the front bump, a mold member surrounding the first
semiconductor chip, the second semiconductor chip, and the carrier
bump, and an external connection bump disposed on the carrier bump.

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FIG. 1