What is claimed is:

1. A semiconductor device, comprising:

a first inter metal dielectric (IMD) layer on a substrate, the first IMD layer including a low-k material having a dielectric constant lower than a dielectric constant of silicon oxide;

a first blocking layer on the first IMD layer, the first blocking layer including an oxide having a dielectric constant higher than the dielectric constant of the first IMD layer, the first blocking layer having no carbon;

a metal wiring through the first IMD layer and the first blocking layer; and

a second blocking layer on the metal wiring and the first blocking layer, the second blocking layer including a nitride, the second blocking layer having no carbon, wherein the second blocking layer partially covers an upper surface of the metal wiring.

2. The semiconductor device of claim 1, wherein the first IMD layer includes silicon oxide including carbon and hydrogen (SiCOH), silicon oxide doped with fluorine (F-SiO2) or a porous silicon oxide.

3. The semiconductor device of claim 2, wherein the first IMD layer includes carbon of about 10% to about 50%.

4. The semiconductor device of any one of claims 1 to 3, wherein a thickness of the first IMD layer is greater than a thickness of the first blocking layer.

5. The semiconductor device of any one of claims 1 to 4, wherein the first blocking layer includes silicon oxide.

6. The semiconductor device of claim 5, wherein the first blocking layer includes silicon oxide formed using TEOS (Tetraethyl orthosilicate) as a source.

7. The semiconductor device of any one of claims 1 to 6, wherein the first blocking layer includes an insulation material having a dielectric constant of about 3.9 to about 4.5.

8. The semiconductor device of any one of claims 1 to 7, wherein the second blocking layer includes an insulation material having a dielectric constant higher than a dielectric constant of the first blocking layer.

9. The semiconductor device of any one of claims 1 to 8, wherein the second blocking layer includes silicon nitride having no carbon.

10. The semiconductor device of any one of claims 1 to 9, wherein the metal wiring includes copper.

11. The semiconductor device of any one of claims 1 to 10, wherein the metal wiring includes a contact plug and a metal pattern on the contact plug, and wherein the first blocking layer contacts on an upper sidewall of the metal pattern.

12. The semiconductor device of any one of claims 1 to 11, further comprising:

a second inter metal dielectric (IMD) layer on the second blocking layer, the second IMD layer including a material having a dielectric constant higher than the dielectric constant of the first IMD layer; and

a via contact contacting on the metal wiring through the second IMD layer and the second blocking layer.

13. The semiconductor device of claim 12, wherein the via contact includes a metal different from a metal of the metal wiring.

14. The semiconductor device of claim 12 or claim 13, further comprising:

an upper metal pattern on the via contact, the upper metal pattern including a metal different from a metal of the metal wiring; and

an upper insulating interlayer covering the upper metal pattern.

15. The semiconductor device of any one of claims 1 to 14, further comprising:

a lower inter metal dielectric (IMD) layer between the substrate and the first IMD layer, the lower IMD layer including a low-k material having a dielectric constant lower than a dielectric constant of silicon oxide; and

at least one of lower wiring structure including a lower metal wiring through the lower IMD layer,

wherein the lower wiring structure are formed on the substrate, and

wherein one lower wiring structure is stacked or a plurality of lower wiring structures are stacked in multiple layers.

16. The semiconductor device of claim 15, further comprising an etch stop layer between lower wiring structures, wherein the etch stop layer is formed on the lower IMD layer and the lower metal wiring, and the etch stop layer includes SiCN.

17. The semiconductor device of claim 15 or claim 16, further comprising:

a lower first blocking layer at ones of portions between the lower wiring structures, wherein the lower first blocking layer is formed on the lower IMD layer and includes oxide having a dielectric constant higher than the dielectric constant of the first IMD layer; and

a lower second blocking layer on the lower metal wiring and the lower first blocking layer, the lower second blocking layer including nitride.

18. A semiconductor device, comprising:

a lower wiring structure including a lower inter metal dielectric (IMD) layer and a lower metal wiring through the lower IMD layer on a substrate, the lower IMD layer including a low-k material having a dielectric constant lower than a dielectric constant of silicon oxide, and the lower metal wiring including a metal;

a first IMD layer on the lower wiring structure, the first IMD layer including a low-k material having a dielectric constant lower than a dielectric constant of silicon oxide;

a metal wiring through the first IMD layer;

a blocking layer structure on the first IMD layer and the metal wiring, the blocking layer structure including a first blocking layer and a second blocking layer, the first blocking layer including a material having a dielectric constant higher than the dielectric constant of the first IMD layer, and the second blocking layer including a material having a dielectric constant higher than the dielectric constant of the first blocking layer, each of the first blocking layer and the second blocking layer having no carbon;

a second IMD layer on the second blocking layer, the second IMD layer including a material having a dielectric constant higher than the dielectric constant of the first IMD layer; and

a via contact on the metal wiring through the second IMD layer and the second blocking layer,

wherein the second blocking layer partially covers an upper surface of the metal wiring.

19. The semiconductor device of claim 18, wherein the first blocking layer includes silicon oxide.

20. A semiconductor device, comprising:

a lower structure including a transistor on a substrate;

a first IMD layer on the lower structure, the first IMD layer including a low-k material having a dielectric constant lower than a dielectric constant of silicon oxide;

a metal wiring through the first IMD layer;

a blocking layer structure on the first IMD layer and the metal wiring, the blocking layer structure including a first blocking layer and a second blocking layer, the first blocking layer including a material having a dielectric constant higher than the dielectric constant of the first IMD layer, and the second blocking layer including a material having a dielectric constant higher than the dielectric constant of the first blocking layer, each of the first blocking layer and the second blocking layer having no carbon;

a second IMD layer on the blocking layer structure;

a via contact on the metal wiring through the second IMD layer and the second blocking layer;

an upper metal pattern on the via contact; and

an upper insulating interlayer covering the upper metal pattern,

wherein the second blocking layer partially covers an upper surface of the metal wiring.