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(54) Title: DYNAMIC POWER SAVING MEMORY ARCHITECTURE

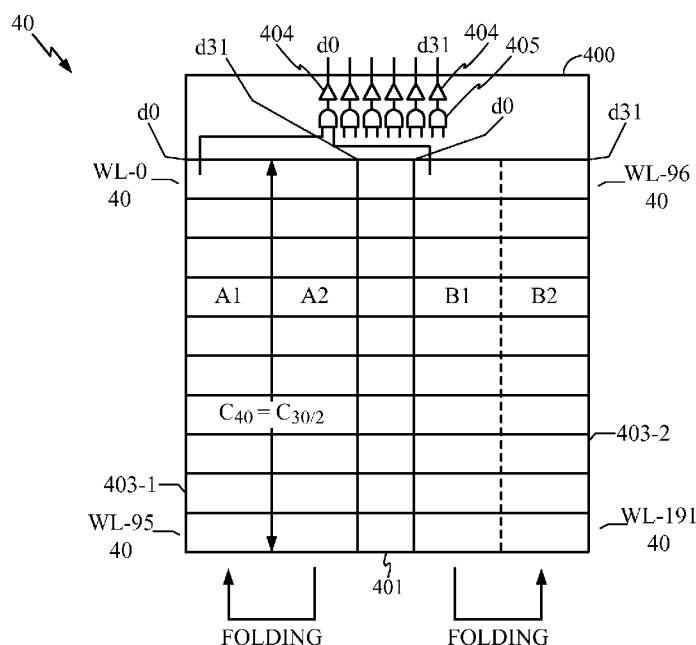


FIG. 4

(57) Abstract: A memory includes multiple interface ports. The memory also includes at least two sub-arrays each having an instance of all of the bit lines of the memory and a portion of the word lines of the memory. The memory has a common decoder coupled to the sub-arrays and configured to control each of the word lines. The memory also includes multiplexers coupled to each of the interface ports. The multiplexers are configured to cause the selection of one of the sub-arrays based upon an address of a memory cell received at one or more of the interface ports.



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