IMPROVED LOW RESISTANCE CONTACTS FOR SEMICONDUCTOR DEVICES

Field of the Invention

[0001] The present invention relates to improvements in low resistance contacts for semiconductor devices. In particular, the present invention relates to a method of providing semiconductor device transistors with improved low resistance contacts.

Background of the Invention

[0002] Germanium (Ge) is a promising material for advanced semiconductor devices, because it provides much higher carrier mobilities than Silicon (Si). A remaining stumbling block to the association of Germanium (Ge) with production processes of advanced logic devices, is the high contact resistance to n-type Ge layers. The performance of Ge and III-V devices can be improved by reducing contact resistance and process variability. High resistance may arise from poor quality contacts, process variability can arise from rough or unintentionally textured surfaces.

[0003] An approach to create stable low resistive contacts is to form a metal–semiconductor alloy, such as NiGe, at the surface in combination with high doping concentrations underneath. Specifically in Ge, the n-type system has proven difficult because of the large electron Schottky barrier height (eSBH) and resulting high contact resistance (ρ_c), and surface states associated with dangling bonds at the Ge surface can lead to Fermi-Level Pinning (FLP) [1, 2]. This can affect metal/Ge contact behaviour, because the Fermi level is pinned close to the valence band.

[0004] Three of the most common n-type Ge contact solutions include (a) ultra-thin amorphous insulating layers to terminate the free dangling bonds and eliminate FLP, (b) surface passivation to bond other impurity species to the dangling Ge bonds at the surface, and (c) optimization of the metal-

semiconductor alloy, such as NiGe, in combination with high active doping concentrations underneath to create stable low-resistive contacts. To form the metal/semiconductor alloy, Ni is deposited, and then an anneal is performed to react the Ni with the Ge. Typically a standard anneal (Rapid-Thermal-Anneal, or RTA) is applied. This results in a relatively rough interface between the NiGe layer and the Ge underneath. The NiGe material is poly-crystalline in nature so it is generally not planar.

[0005] Theoretical studies have shown that a thin insulating tunnel barrier can de-pin the Ge surface with optimum thicknesses of approximately 1 nm [4]. Selenium segregation was recently used to reduce eSBH for NiGe/n-Ge contacts [5], while CF_4 plasma treatment of the Ge surface was experimentally demonstrated to alleviate FLP [6]. Gallacher *et al.* extracted specific contact resistivity (ρ_c) of 2.3×10^{-7} $\Omega.cm^2$ on n-type Ge that was doped during epitaxial growth [7]. The optimum NiGe formation temperature was a 340 °C Rapid Thermal Anneal (RTA). However, the NiGe interface with the underlying substrate was not smooth.

[0006] Laser-Thermal-Annealing (LTA) techniques are of increasing interest in semiconductor processing, as it enables ultrafast annealing with very limited thermal budgets. It can suppress dopant diffusion and generates high levels of dopant activation. Specifically in Ge, Mazzocchi *et al.* reported high activation levels of B and P dopants ($>1\times10^{20}$ cm^{-3}) as well as limited diffusion when they used LTA with energy densities in the range of 0.57-1.8 J/cm^2 [8]. High quality n^+/p junctions were also realized using LTA of Sb-doped Ge by Thareja *et al.* [9]. Furthermore, Firrincieli *et al.* reported ρ_c of 8×10^{-7} $\Omega.cm^2$ on n-type Ge where LTA was used for dopant activation, in combination with RTA for NiGe formation [10]. The NiGe layers were thermally stable up to 350 °C, but the interface with the Ge substrate was not flat. This is common for NiGe layers formed by RTA. Another example is disclosed in a paper by LIM P S Y et al entitled 'Fermi-level depinning at the metal-germanium interface by the formation of epitaxial nickel digermanide NiGe2 using pulsed laser anneal' – Applied

Physics Letters American Institute of Physics USA, col. 101, no 17, 22 October 2012.

[0007] An improved method of providing semiconductor devices with low resistance contacts is therefore required, which mitigates at least the above shortcomings of the prior art.

Summary of the Invention

[0008] According to the invention there is provided, as set out in the appended claims, a method of forming at least one Metal Germanide contact on a substrate, for example a Germanium (Ge) or Silicon (Si) substrate, for providing a semiconducting device (100), comprising the steps of:

providing a first layer (120) of Germanium (Ge);

providing a second layer of metal; and

reacting the second layer with the first layer with high energy density pulses for obtaining a Germanide metal layer (160A) having a substantially planar interface with the underlying first (Ge) layer.

[0009] In the context of the present invention the term 'substrate' should be afforded a broad definition. The substrate refers to the part of the wafer where integrated circuits and transistors and other semiconductor devices can be located. In other cases 'substrate' can refer to the entire thickness of the wafer. In one embodiment Germanium is likely to be integrated on top of Silicon wafers (used for mechanical strength), so in that sense the germanium can be described as a "layer".

[00010] In one embodiment the high energy density pulses are in the range 0.25 to 0.55 J/cm^2 and pulse durations generate a temperature of at least 800°C.

[00011] In one embodiment the inventors have used LTA for NiGe contact formation on n-type Ge substrates, and compared same systematically to

results generated by conventional RTA with respect to surface topography, interface quality, crystal structure, material stoichiometry, specific contact resistivity, and thermal stability. Germanide layers formed by LTA are referred to herein as Ni_xGe_y, because it will be demonstrated that there are multiple stoichiometries present under processing conditions. It will be appreciated that one important advantage of using LTA with process conditions as claimed is that it allows annealing in ambient air thus simplifying the conditions for the overall process.

[00012] In one embodiment the metal comprises Nickel (Ni).

[00013] In one embodiment the metal comprises at least one of: Fe, Co, Ni, Pd, Pt, Cu or Yb.

[00014] In one embodiment the temperature generated is at least 900°C.

[00015] In one embodiment the temperature generated is below 1500°C.

[00016] In one embodiment the temperature generated is in the range of 930 °C and 1460 °C.

[00017] In one embodiment the pulse length is above 25 nanoseconds.

[00018] In one embodiment the pulse length is between 50 nanoseconds and 1 microsecond.

[00019] In one embodiment the pulse length is between 50 nanoseconds and 500 nanoseconds.

[00020] According to an aspect of the present invention there is therefore provided a method of forming at least one Germanide (Ni_xGe_y) contact on a Germanium (Ge) substrate for providing a semiconducting device (100), comprising the steps of providing a first layer (120) of Germanium (Ge) with well and dopant implants; activating dopants with a heat treatment; providing a second layer of Nickel (Ni); and reacting the second layer with the first layer with high energy density pulses for obtaining a Germanide (Ni_xGe_y) layer (160A) having a substantially planar interface with the underlying first (Ge) layer.

[00021] Forming the NiGe layer using tuned laser anneal conditions advantageously forms a substantially flat interface between the NiGe layer and the Ge underneath. The laser anneal is a relatively short pulse of high energy density, which temporarily melts the top Ge surface of the wafer, while the Ni is unmelted. Ge melts ~936 °C, while Ni melts ~1455 °C. The surface temperature during the LTA process lies somewhere in that range. The solubility of Ni in Ge is vastly greater in the liquid Ge phase, compared to the solid Ge phase, and thus rapidly dissolves into that liquid layer. In effect the liquid Ge consumes the Ni on top very quickly. In comparison in the standard rap-id-thermal-anneal case Ni is in contact with solid Ge and there is a slower solid-solid reaction Moreover, the penetration depth of the laser pulse is limited whereby, advantageously, the heat travels only a certain distance from the top of the wafer downwards, contrarily to a conventional furnace-based or RTA-based method in which the entire wafer experiences the temperature within a tool chamber. Furthermore the energy density of the laser anneal process can tailor the melt depth at the Ge surface, and thus control the thickness of the nickel-germanide layer that is formed. There are many ways to thermally treat semiconductors, however laser thermal annealing provides a very localised treatment, both in terms of time (ns) and in terms of location on the substrate, i.e. typically just the surface layers are treated. It is envisaged that other thermal anneal techniques can be used.

[00022] In an embodiment of the method according to the invention, the first layer is a n-type wafer (100) having a resistivity exceeding 40 Ω·cm.

[00023] In an embodiment of the method according to the invention, the step of providing the second layer of Nickel (Ni) further comprises depositing the Nickel (Ni) material by thermal evaporation.

[00024] In an embodiment of the method according to the invention, the method may comprise the further step of TLM patterning and dry etching for minimizing leakage currents.

[00025] In an embodiment of the method according to the invention, the high energy density pulses are provided by a laser source in a laser thermal annealing (LTA) treatment. In a variant of this embodiment, the LTA treatment is a single-pulse treatment at λ= 308 nm, with laser densities in the range 0.25 to 0.55 J/cm^2 and pulse durations in the range 144 to 165 ns. In a further variant of this embodiment, laser densities are preferably in the range 0.35 to 0.45 J/cm^2. The laser beam preferably has an area of substantially 10×10 mm^2. It will be appreciated that other wavelengths can be used, for example using an Excimer laser

[00026] According to another aspect of the present invention, there is also provided a semiconductor device (100) comprising at least one n-channel transistor, wherein the or each n-channel transistor comprises a semiconductor region (120) comprised of germanium (Ge); a gate electrode (110) formed on the semiconductor region via a gate insulation film (140); and junction regions (160) formed in the semiconductor region on both sides of the gate electrode, wherein each region is made of nickel (Ni) reacted with the semiconductor region (Ge). The device is characterised in that the nickel (Ni) is reacted with the germanium (Ge) region with high energy density pulses, whereby each region (Ni_xGe_y) has a substantially planar interface with the underlying semiconductor region (120).

[00027] In an embodiment of the device according to the invention, the semiconductor region is a n-type wafer (100) having a resistivity exceeding 40 Ω·cm.

[00028] In an embodiment of the device according to the invention, the high energy density pulses are provided by a laser source in a laser thermal annealing (LTA) treatment. In a variant of this embodiment, the LTA treatment is a single-pulse treatment at λ= 308 nm, with laser densities in the range 0.25 to 0.55 J/cm^2 and pulse durations in the range 144 to 165 ns. In a further variant of this embodiment, the laser densities are preferably in the range 0.35 to 0.45 J/cm^2. The laser beam preferably has an area of substantially 10×10 mm^2.

[00029] In one embodiment there is provided a method for forming metal germanide comprising

depositing a metal layer on a germanium layer;

heating the metal layer with a laser source;

characterized in that the heating occurs at a temperature of at least 800°C.

[00030] In one embodiment the heating is pulsed.

[00031] In one embodiment the high energy density pulses are in the range 0.25 to 0.55 J/cm^2 and pulse durations generate a temperature of at least 800°C.

Brief Description of the Drawings

[00032] For a better understanding of the invention and to show how the same may be carried into effect, there will now be described by way of example only, specific embodiments, methods and processes according to the present invention with reference to the accompanying drawings in which:

[00033] Figure 1 shows procedural steps of a first embodiment of a method according to the invention, the testing of which has yielded the respective subject-matter of each of remaining Figures 2 to 10.

[00034] Figure 2 shows AFM images of Germanide layers respectively formed by (a) RTA conventionally and by (b) LTA according to the method of Figure 1, and wherein a table shows surface roughness data for RTA and LTA samples.

[00035] Figure 3A shows a XTEM image of a NiGe layer conventionally formed by RTA at 350 °C.

[00036] Figure 3B shows a XTEM image of a Ni_xGe_y layer formed by 0.35 J/cm^2 LTA according to the method of Figure 1, having a smoother Ge-substrate interface relative to the interface of Figure 3A.

[00037] Figure 4A shows both a HRXTEM image of the interface between the Ge and the NiGe after the RTA of Figure 3A, having a substantial transition region, and an inset image showing the diffraction patterns from Ge and NiGe.

[00038] Figure 4A shows both a HRXTEM image of the interface between the Ge and the Ni_xGe_y. after the LTA of Figure 3B, having a substantially sharper interface, and an inset image showing the diffraction patterns from Ge and Ni_xGe_y.

[00039] Figure 5 shows representative XTEM images of the Ni_xGe_y-substrate layer and the interface between the Ge and the Ni_xGe_y, where a high energy density of substantially 0.55 J/cm^2 LTA was applied, and wherein larger grains can be seen in the Ni_xGe_y layer, and the interface is not as sharp as in Figures 3B and 4B.

[00040] Figure 6 charts resistance versus contact spacing for both conventional RTA samples and LTA samples according to the method of Figure 1, wherein the inset graph shows I-V characteristics of a typical TLM structure in which Ni_xGe_y contacts are formed by LTA at an energy of 0.45 J/cm^2.

[00041] Figure 7 charts ρ_c versus R_{sh} for a plurality of samples, including NiGe on n-type Ge using RTA, which shows that, for a fixed R_{sh}, LTA can produce better ρ_c, if a correct energy density condition is selected.

[00042] Figure 8 charts resistance versus contact spacing after post-processing RTA treatments for which anneal times were 30 seconds. Germanide contact was initially formed by LTA with energy of 0.45 J/cm^2.

[00043] Figure 9 charts ρ_c versus post-processing RTA treatments, in which only one sample was post-processed for RTA and for LTA, whereby the post-processing thermal-budget should be considered as cumulative.

[00044] Figure 10 shows a semiconductor device according to one embodiment of the invention.

Detailed Description of the Embodiments

[00045] There will now be described by way of example a specific mode contemplated by the inventors. In the following description numerous specific details are set forth in order to provide a thorough understanding. It will be apparent however, to one skilled in the art, that the present invention may be practiced without limitation to these specific details. In other instances, well known methods and structures have not been described in detail so as not to unnecessarily obscure the description.

[00046] Laser Thermal Annealing (LTA) is used to form Germanide contacts on n-doped Ge, which are systematically compared to results generated by conventional rapid thermal annealing (RTA). Surface topography, interface

quality, crystal structure, and material stoichiometry are explored for both annealing techniques. For electrical characterization, specific contact resistivity and thermal stability are extracted. It is shown that LTA can produce a uniform contact with a remarkably smooth substrate interface, with specific contact resistivity 2 to 3 orders of magnitude lower than with the RTA technique. It is shown that a specific contact resistivity of 2.84×10^{-7} $\Omega.cm^2$ is achieved for optimized LTA energy density conditions.

[00047] Figure 1 summarizes the process undertaken, from which the following results are discussed in this study. After cleaning, high-resistivity (>40 Ω·cm) n-type (100) wafers received well implants, namely P with the dose of 4×10^{12} cm^{-2} and energy of 180 keV, followed by a B implant with the dose of 1×10^{13} cm^{-2} and energy of 40 keV to create a semi-insulating layer. The wafers then received a shallow P implant with the dose of 1×10^{15} cm^{-2} and energy of 12 keV. Dopant activation was performed using an RTA at 500 °C for 10 seconds in an N_2 ambient. Thereafter 20 nm of Ni was deposited using thermal evaporation. TLM patterning and dry etch was then carried out to minimize leakage currents. Nickel is described herein to illustrate operation of the invention, it will be appreciated that other metals can be used such as Fe, Co, Ni, Pd, Pt, Cu or Yb.

[00048] One set of samples received RTA treatment at either 250, 275, 300, 325 or 350 °C in N_2 for 30 seconds. Another set of samples received LTA processing (λ= 308 nm, single-pulse) with laser densities ranging from 0.25 to 0.55 J/cm^2 and time durations ranging from 144 to 165 ns. The laser beam area was approximately 10×10 mm^2. It is noted that these energy densities are significantly lower than those required for proper LTA assisted dopant activation in Ge [8].

[00049] Various material characterization techniques were applied to inspect NiGe layer surface topography and crystalline quality, including scanning electron microscopy (SEM), atomic force microscopy (AFM), x-ray diffraction (XRD), and cross-sectional transmission electron microscopy (XTEM). XTEM was

carried out using the JEOL 2100 high-resolution TEM. In particular, AFM shows smoother surface layer, and cross-sectional TEM shows a sharp, *non*-undulating interface after LTA. For electrical characterization, the Transfer Length Method (TLM) was used to extract ρ_c and the KEITHLEY 37100 and KEITHLEY 2602 were used. In particular, contact resistance is determined as approximately 100 times lower using LTA, relative to RTA.

[00050] In order to study the respective effects of RTA and LTA, firstly surface roughness was evaluated. AFM was performed in tapping/non contact mode at room temperature in air. Figure 2 shows representative AFM images of NiGe surface topography which were formed by (a) RTA at 275 °C and (b) LTA at the energy of 0.35 J/cm^2. Surface roughness (RMS) for the RTA sample is approximately 1.28 nm whereas the LTA treated sample exhibits a roughness of approximately 0.39 nm. The table in Figure 2 shows the RMS data extracted for all the samples. RMS is larger for the RTA set, except for the highest energy density LTA.

[00051] Much like there is a process window for NiGe formation by RTA [11, 12] where, at high temperatures, the thin film agglomerates into islands, this data indicates that LTA also has a process window for Ni_xGe_y formation, above which the film degrades. 0.55 J/cm^2 appears too elevated a value for this application. Mazzocchi *et al.* also reported a change in AFM RMS versus energy density in their LTA dopant activation study in Ge, which was attributed to the transition from non-melt, to sub-melt, to melt conditions [8]. From Figure 2 therefore, it can be concluded that Ni_xGe_y layers formed by LTA, at an energy density of 0.25 to 0.45 J/cm^2, are much smoother that those formed by RTA.

[00052] A representative XTEM image from a Germanide contact formed by RTA at 350 °C for 30 seconds in N_2 is shown in Figure 3A. As seen in the figure, large grains of NiGe are formed, with a rough undulating interface between the alloy and the Ge substrate. This result is expected, as non-smooth NiGe interfaces are commonplace when RTA is used for the formation anneal [5,

7, 13]. With comparative reference to Figure 3B now, the representative XTEM image of a sample treated by LTA, in this case with an energy density of 0.35 J/cm^2 stands in stark contrast, as LTA results in smaller polycrystalline grains of Germanide and a very a flat interface between the Ge substrate and the alloy.

[00053] A representative high-resolution (HR) XTEM image of the Germanide-substrate interface in the sample of Figure 3A is next shown in Figure 4A. As seen in the figure, there is no sharp transition from Ge to NiGe. With comparative reference to Figure 4B now, the representative (HR) XTEM image of a sample treated by LTA, in this case with an energy density of 0.35 J/cm^2 stands in stark contrast, showing a flat and uniform interface between Ge and the Germanide.

[00054] The rows of Ge atoms are clearly observable in the substrate. In terms of the interface quality, the interface is substantially planar and the term "atomically-flat" may be used, because there are unbroken horizontal rows in the Ge (100) substrate transitioning immediately to Germanide above it, without any detectable interfacial region or transition zone. Furthermore, the evidence of (HR) TEM indicates that this Germanide layer is not necessarily lattice matched, nor epitaxially grown on top of the Ge substrate. If one follows any row of Ge substrate atoms diagonally upwards in Figure 4B, this sequence does not continue into the Germanide layer. The rows of atoms in the Germanide layers are arranged in different directions to those in the (100) Ge substrate. In some regions of the Ge substrate-germanide interface the is evidence of an epitaxial relationship between the two crystalline materials, but this is highly localised to certain places along the horizontal interface. Furthermore due to lattice mismatch between the two materials and the small size of crystals in the germanide layer, this does not extend vertically throughout the entire germanide layer. Lattice-matched NiSi growth on Si has been reported by Gao *et al.*, where ultra-thin Ni layers were deposited on Si [14], and $NiSi_2$ preferentially formed as it has a similar lattice spacing to Si.

[00055] The dramatic improvement in interface roughness is linked to the thermal gradient and shallow heat distribution associated with ultra-short-pulse LTA. Unlike RTA, wherein substantially the entire sample is at the target temperature without significant thermal gradients, LTA generates intense thermal gradients, linked to the wavelength of the incident energy pulse, and the thermal diffusivity of the target material. The LTA pulse heats the surface locally, and may melt the surface layers depending on the energy density applied. The two inset pictures in Figure 4B show the electron diffraction pattern of Ge substrate (bottom right) and the Ni_xGe_y (top right).

[00056] With reference to Figure 5 next, XTEM images are presented for LTA at a high energy density of 0.55 J/cm^2. The left section (a) of Figure 5 is a wide view, and the right section (b) is a high resolution view, of Ge and the contact interface. In this case, larger grains of Germanide are formed and the interface is coarser relative to those observable in Figures 3B and 4B.

[00057] Turning now to electrical characterisation, using the fabricated TLM test structures, ρ_c of the germanide/n-type Ge interface and the sheet resistance R_{sh} of the underlying P doped Ge layer were then extracted. In the TLM test structure, each NiGe bar was 380× 100 μm^2 and the spacings were 4, 16, 36, 64, 100, 144, and 196 μm. The layout consisted of a repeated array of this TLM design. Approximately 40 TLM structures within each array were electrically measured in order to extract reliable values for ρ_c and R_{sh}.

[00058] Figure 6 shows the output from a TLM measurement in the above context. The inset shows current versus voltage as a function of contact spacing of a typical TLM structure fabricated using LTA (0.45 J/cm^2). The resistance between contacts increases as the spacing increases. In the main part of Figure 6, resistance versus contact spacing is plotted for the NiGe formed by RTA at 275°, 300°, 350 °C and LTA at 0.35, 0.45, and 0.55 J/cm^2. Straight lines are fitted to the data. Intercepts of the line with vertical and horizontal axes are

used to calculate ρ_c and R_{sh} according to theory [3]. The following table shows the results of ρ_c and R_{sh} extracted from all the TLM measurements.

Contact formation	R_{sh}(Ω/sq)	ρ_c (Ω.cm^2)
275 °C	196.1	6.31×10^{-4}
300 °C	186.0	1.61×10^{-4}
325 °C	216.3	9.57×10^{-4}
350 °C	161.3	1.35×10^{-4}
0.35 J/cm^2	163.6	1.33×10^{-6}
0.45 J/cm^2	147.0	2.84×10^{-7}
0.55 J/cm^2	190.7	8.45×10^{-4}

[00059] In the RTA samples, R_{sh} and ρ_c decrease as the formation temperature increases from 275 to 350 °C, except at 325 °C for which there is currently no physical explanation. In an overall sense, the RTA samples produce $\rho_c > 10^{-4}$ Ω.cm^2. In general, R_{sh} and ρ_c are lower in the LTA samples. The best ρ_c value is 2.84×10^{-7} Ω.cm^2 obtained for the TLM sample LTA-annealed at 0.45 J/cm^2, and $\rho_c = 1.33 \times 10^{-6}$ Ω.cm^2 obtained for the TLM sample LTA-annealed at 0.35 J/cm^2 is also a significant result. These ρ_c values are 2 to 3 orders of magnitude lower than the equivalent RTA cases. It should be noted that the only process variable in this experimental work was the NiGe formation anneal, and it is interesting to see that increasing the LTA energy density to 0.55 J/cm^2 results in higher ρ_c, which may be attributed to the degradation of the interface quality seen as shown in Figure 5.

[00060] It is well-known that ρ_c is a strong function of active doping in the substrate below the contact, thus any boost in dopant activation will yield a similar improvement in ρ_c. With reference to the above results the 0.35 and 0.45 J/cm^2 LTA, it may be argued that the LTA is merely improving the P activation which is generating these ρ_c results. From the above table, the R_{sh} values suggest that LTA is a benefit for P activation. However, with reference now to Figure 7, plotting ρ_c versus R_{sh} shows that, for a fixed R_{sh}, LTA can still produce better ρ_c, if the correct energy density condition is selected.

[00061] Thermal stability of the Ni_xGe_y layers was also analysed. The ultra-short time and highly-localized energy densities of LTA processing may form highly non-equilibrium metastable conditions in the semiconductor materials and substrates. In such a case, the thermal budget in the processes which follow the LTA process step, may cause any metastable condition to revert back to a more equilibrium state. In order to evaluate Germanide thermal stability, a sample prepared at 300 °C RTA and a sample prepared by 0.45 J/cm^2 LTA were subjected to "post-processing" RTA treatments from 100 to 500 °C. The anneal times were 30 seconds each. Only one sample was post-processed for both RTA and LTA, whereby the post-processing thermal-budget should be considered as cumulative in this analysis. Figure 8 provides TLM measurements of the LTA sample after post-processing RTA steps, which show that the slope and intercept of the fitted lines are changing after each RTA treatment, indicating that R_{sh} and ρ_c are deteriorated. Some TLM measurements are not shown in Figure 8, however, for purposes of not obscuring the Figure unnecessarily.

[00062] Extracted ρ_c results are shown in Figure 9. In the LTA sample, ρ_c increases gradually, and at 250 °C there is a significant increase in resistivity. By 500 °C, the ρ_c value is similar to the RTA cases. In the RTA sample, ρ_c shows a slight decrease at 150 °C, then follows an increasing trend. Both samples were inspected by SEM (data not shown), and it was observed at the end of this post-processing anneal sequence that the Germanide had agglomerated. It is well known that NiGe layers annealed at 500 °C become agglomerated [11, 12].

[00063] There are various known methods for altering thermal stability of Silicide or Germanide layers. One recent report highlighted the benefit of co-sputtering Ni and Pt prior to alloy formation [14]. In that reference, the addition of Pt improved the thermal stability of R_{sh} in the Germanide layers, and alternative embodiments of the present method may therefore include the addition of Pt to achieve the same benefit.

[00064] The present invention thus provides an improved method of forming Germanide (Ni_xGe_y) contacts on n-type Germanium (Ge) substrates for use with semiconducting devices, with a substantially planar, or regular, interface relative to the rough, uneven interface of prior art techniques. The quality of Germanide contacts formed by state-of-the-art LTA on n-type Ge was investigated and compared systematically with conventional RTA. LTA resulted in smoother layers, smaller polycrystalline grains, and greater content of Ni-rich Germanide phases. The Germanide-substrate interface was dramatically sharpened without any detectable interfacial region or transition zone in HRXTEM. ρ_c of the contacts was also extracted from TLM structures. The best contact resistivity obtained was 2.84×10^{-7} $\Omega.cm^2$ using a 1×10^{15} cm^{-2} 12 keV P implant followed by 500 °C 10-second activation anneal and LTA of 0.45 J/cm^2 energy density for Germanide formation.

[00065] It will therefore be readily understood by the skilled reader that the LTA annealing technique disclosed herein is particularly advantageous for any semiconductor device having a Ge or GaAs component such as, typically, but non-exhaustively, CMOS devices, photodiodes and imagers. With reference to Figure 10, a semiconductor device 100 is shown by way of example, with which the invention may be practiced. The semiconductor device 100 has a gate electrode 110 formed over a Ge substrate 120, having an n- or p-well 130 with a gate insulating film 140 formed between the well and the gate. A sidewall 150 is formed about the gate insulting film 140 and the gate electrode 110. An Ni_xGe_y layer 160 is formed on both sides of the gate electrode 110 as respective junctions, on the sides of which the sidewall 150 is formed and, in the Figure and by way of illustration only, the left layer 160A is an Ni_xGe_y layer formed by LTA according to the invention, and the right layer 160B is an NiGe layer formed by RTA according to the prior art.

[00066] It will be appreciated that use of any of the above methods can be employed in manufacturing germanium or III-IV semiconductor devices, such as transistor devices.

[00067] It will be appreciated that use of any of the above methods can be employed in manufacturing of contact structures of germanium or III-IV semiconductor devices.

[00068] In the specification the terms "comprise, comprises, comprised and comprising" or any variation thereof and the terms include, includes, included and including" or any variation thereof are considered to be totally interchangeable and they should all be afforded the widest possible interpretation and vice versa.

[00069] The invention is not limited to the embodiments hereinbefore described but may be varied in both construction and detail.

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Claims

1. A method of forming at least one Metal Germanide contact on a substrate for providing a semiconducting device (100), comprising the steps of

providing a first layer (120) of Germanium (Ge);

providing a second layer of metal; and

reacting the second layer with the first layer with high energy density pulses for obtaining a Germanide metal layer (160A) having a substantially planar interface with the underlying first (Ge) layer, wherein the high energy density pulses are in the range 0.25 to 0.55 J/cm^2 and pulse durations generate a temperature of at least 800° C.

2. The method according to claim 1, wherein the metal comprises Nickel (Ni).

3. The method according to claim 1, wherein the metal comprises at least one of: Fe, Co, Ni, Pd, Pt, Cu or Yb.

4. The method according to claim 1 wherein the temperature generated is at least 900° C.

5. The method according to claim 1 wherein the temperature generated is below 1500° C.

6. The method according to claim 1 wherein the temperature generated is in the range of 930 ° C and 1460 ° C.

7. The method according to claim 1 wherein the pulse length is above 25 nanoseconds.

8. The method according to claim 1 wherein the pulse length is between 50 nanoseconds and 1 microsecond.

9. The method according to claim 8 wherein the pulse length is between 50 nanoseconds and 500 nanoseconds.

10. The method according to claim 1 wherein the first layer is a n-type or p-type wafer (100) having a resistivity greater than 0.001 Ω.cm.

11. The method according to claim 2, wherein the step of providing the second layer of Nickel (Ni) further comprises depositing the Nickel (Ni) material by thermal evaporation.

12. The method according to claim 1, comprising the further step of TLM patterning and dry etching for minimizing leakage currents.

13. The method according to claim 1, wherein the high energy density pulses are provided by a laser source in a laser thermal annealing (LTA) treatment.

14. The method according to claim 13, wherein the LTA treatment is a single-pulse treatment at λ=308 nm, with pulse durations in the range 144 to 165 ns.

15. A semiconductor device manufactured according to the method of claim 1.