Claims

1. A method for the processing of a crystalline silicon device, having a plurality of crystalline silicon regions, at least one crystalline silicon region having a plurality of crystallographic defects or contaminants, the at least one crystalline silicon region being a doped crystalline silicon region in which some dopant atoms are deactivated by combining with a hydrogen atom, the method comprising:

reactivating some of the deactivated dopant atoms by heating and illuminating the doped crystalline silicon region to break at least some of the bonds between dopant atoms and hydrogen atoms while maintaining conditions to create a relatively high concentration of neutral hydrogen atoms whereby some of the hydrogen atoms diffuse from the doped crystalline silicon region without re-bonding to the dopant atoms; and

subsequently heating and illuminating at least a portion of the doped crystalline silicon region to bond some or all of the neutral hydrogen atoms to the crystallographic defects or contaminants.

2. The method as claimed in claim 1 wherein after heating and illuminating the doped crystalline silicon region, a cooling period is provided during which the illumination is maintained to maintain the high concentration of neutral hydrogen atoms.

3. The method of claim 1 or 2 wherein the doped crystalline silicon region is a surface region of the device.

4. The method of claim 1, 2 or 3 wherein some or all of the deactivated dopant atoms are subsequently reactivated by subjecting the doped crystalline silicon region to heat in the presence of illumination.

5. The method of claim 4 wherein the doped crystalline silicon region is allowed to cool in the presence of illumination.

6. The method as claimed in any one of the preceding claims wherein the heating and illumination of the dopant atoms is performed with a laser.

7. The method of claim 1, 2 or 3 wherein some or all of the deactivated dopant atoms in a selected crystalline silicon region are subsequently reactivated by subjecting the dopant atoms in the selected crystalline silicon region to heat and illuminating a crystalline silicon region adjacent to the selected crystalline silicon region whereby electron hole pairs are generated to increase the proportion of minority carriers in the crystalline silicon region

adjacent to the selected crystalline silicon region and such that the minority carriers generated in the region adjacent to the selected crystalline silicon region will diffuse to the selected crystalline silicon region.

8. The method of claim 7 wherein the selected crystalline silicon region is allowed to cool to below 120°C within a carrier lifetime of the minority carriers or within a life expectancy of neutral hydrogen atom or a hydrogen atom of the same charge state as the dopant atoms in the selected crystalline silicon region.

9. The method as claimed in claim 7 or 8 wherein the heating and/or illumination of the selected crystalline silicon region and the crystalline silicon region adjacent to the selected region is performed with a laser.

10. The method as claimed in claim 6 or 9 wherein the laser is scanned over a plurality of crystalline silicon regions to process a larger area of the crystalline silicon device.

11. The method as claimed in any one of the preceding claims wherein hydrogen atoms are introduced into the crystalline silicon by forming a dielectric hydrogen source on a surface of the crystalline silicon and subsequently heating the device to migrate the hydrogen atoms into the crystalline silicon.

12. The method as claimed in claim 11 wherein hydrogen atoms are introduced into the crystalline silicon device from the dielectric hydrogen source to deactivate dopant atoms in surface regions of the crystalline silicon, by heating the device in the absence of illumination or in low illumination conditions.

13. The method as claimed in claim 11 or 12 wherein dielectric hydrogen sources are formed on each of a front and a rear crystalline silicon surface of the crystalline silicon device.

14. The method as claimed in any one of claims 11 to 14 wherein the dielectric hydrogen source comprises a layer or layers of one or more of silicon nitride, amorphous silicon, silicon oxynitride, aluminium oxides.

15. The method as claimed in any one of claims 11 to 14 wherein the crystalline silicon device comprises a crystalline silicon surface n-type diffused layer through which hydrogen must diffuse, the crystalline silicon surface n-type diffused layer having a net active doping concentration of $1x10^{20}$ atoms/cm^3 or less.

16. The method as claimed in any one of claims 11 to 15 wherein the crystalline silicon device comprises a crystalline silicon surface diffused p-type layer through which hydrogen must diffuse, the crystalline silicon surface n-type diffused layer having a net active doping concentration of $1x10^{19}$ atoms/cm^3 or less.

17. The method as claimed in any one of the preceding claims wherein the heating of the crystalline silicon device comprises heating at least a crystalline silicon region of the device to at least 40°C while simultaneously illuminating at least some of the crystalline silicon device with at least one light source whereby the cumulative power of all the incident photons with sufficient energy to generate electron hole pairs within the crystalline silicon device is at least 20mW/cm^2.

18. The method as claimed in any one of the preceding claims wherein the illumination of the crystalline silicon device is from at least one light source and is provided at a level whereby the cumulative power of all the incident photons with sufficient energy to generate electron hole pairs within the crystalline silicon device is at least 50 mW/cm^2, or 60 mW/cm^2, or 70 mW/cm^2, or 80 mW/cm^2, or 90 mW/cm^2, or 100 mW/cm^2, or 150 mW/cm^2, 200 mW/cm^2, or 300 mW/cm^2, or 400 mW/cm^2, or 500 mW/cm^2, or 600 mW/cm^2, or 700 mW/cm^2, or 800 mW/cm^2, or 900 mW/cm^2, or 1000 mW/cm^2, or 1500 mW/cm^2, 2000 mW/cm^2, or 3000 mW/cm^2, or 5000 mW/cm^2, or 10000 mW/cm^2, or 15000 mW/cm^2, or 20000 mW/cm^2, or up to a light intensity at which crystalline silicon begins to melt.

19. The method as claimed in any one of the preceding claims wherein for each of the ranges of cumulative power, the heating of the device comprises heating at least a region of the device to at least 100°C, or to at least 180°C, or to at least 200 °C, or to at least 400 °C.

20. The method as claimed in any one of the preceding claims wherein heating of the crystalline silicon device comprises heating the device to at least 500°C, or to at least 600°C, or to at least 700°C, or to at least 800°C, or to at least 900°C, or to at least 1,000°C, or to at least 1,200°C or to a temperature at which crystalline silicon begins to melt.

21. The method as claimed in any one of the preceding claims wherein heating of the crystalline silicon device is followed by cooling the crystalline silicon device while simultaneously illuminating at least some of the crystalline silicon device with at least one light source whereby the cumulative power of all the incident photons with sufficient energy to generate electron hole pairs within the crystalline silicon device is at least 20mW/cm^2.

22. The method as claimed in any one of the preceding claims wherein a minority carrier concentration is controlled, through the use of light and heat, during a cool-down period after heating, and any post hydrogenation thermal processes, to maintain hydrogen charge states during cool-down to minimise reactivation of defects to which a hydrogen atom has previously bound.

23. The method as claimed in any one of the preceding claims wherein a source of illumination applied to the crystalline silicon device is an array of LEDs or one or more infrared lamps.

24. The method as claimed in any one of the preceding claims wherein the illumination applied to the crystalline silicon device is pulsed.

25. The method as claimed in any one of the preceding claims wherein the intensity of illumination applied to the crystalline silicon device is controlled to maintain the Fermi level at a value of 0.10 to 0.22ev above mid-gap.

26. The method as claimed in any one of the preceding claims wherein the crystalline silicon device comprises a photovoltaic device having at least one rectifying junction.

27. The method as claimed in any one of the preceding claims wherein the doped crystalline silicon region is doped with a p-type (valency 3) dopant selected from boron, aluminium or gallium.

28. The method as claimed in any one of claims 1 to 32 wherein the doped crystalline silicon region is doped with boron and/or phosphorus.