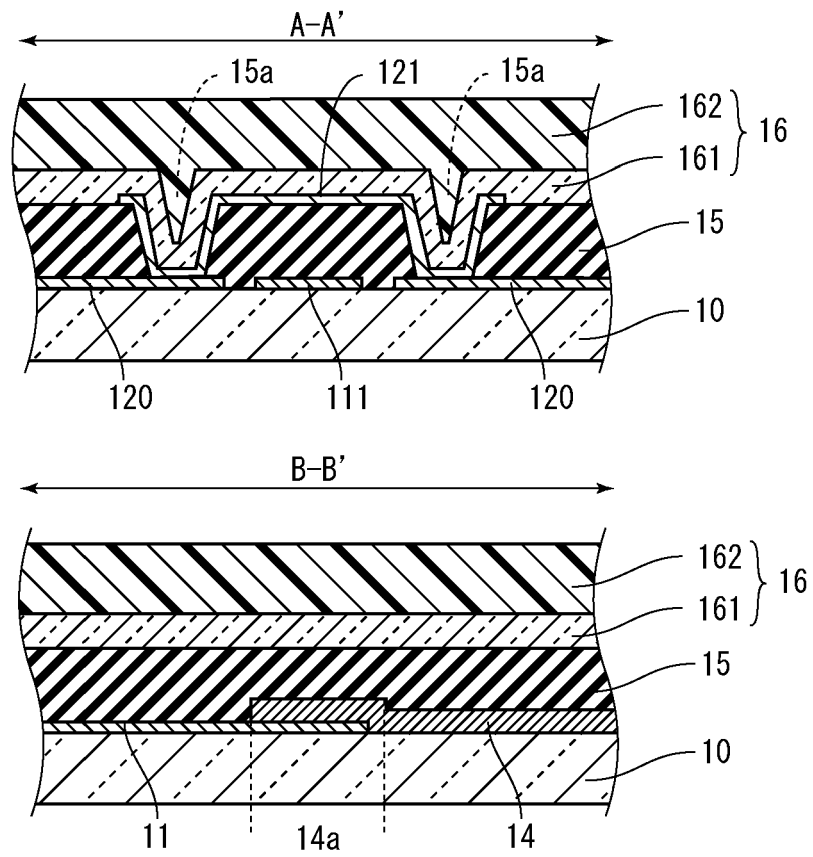
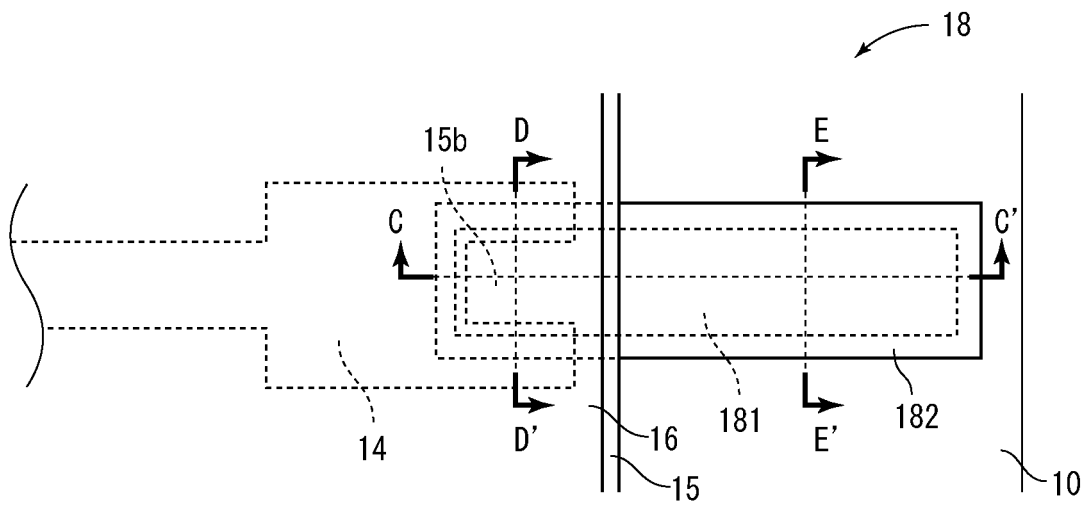


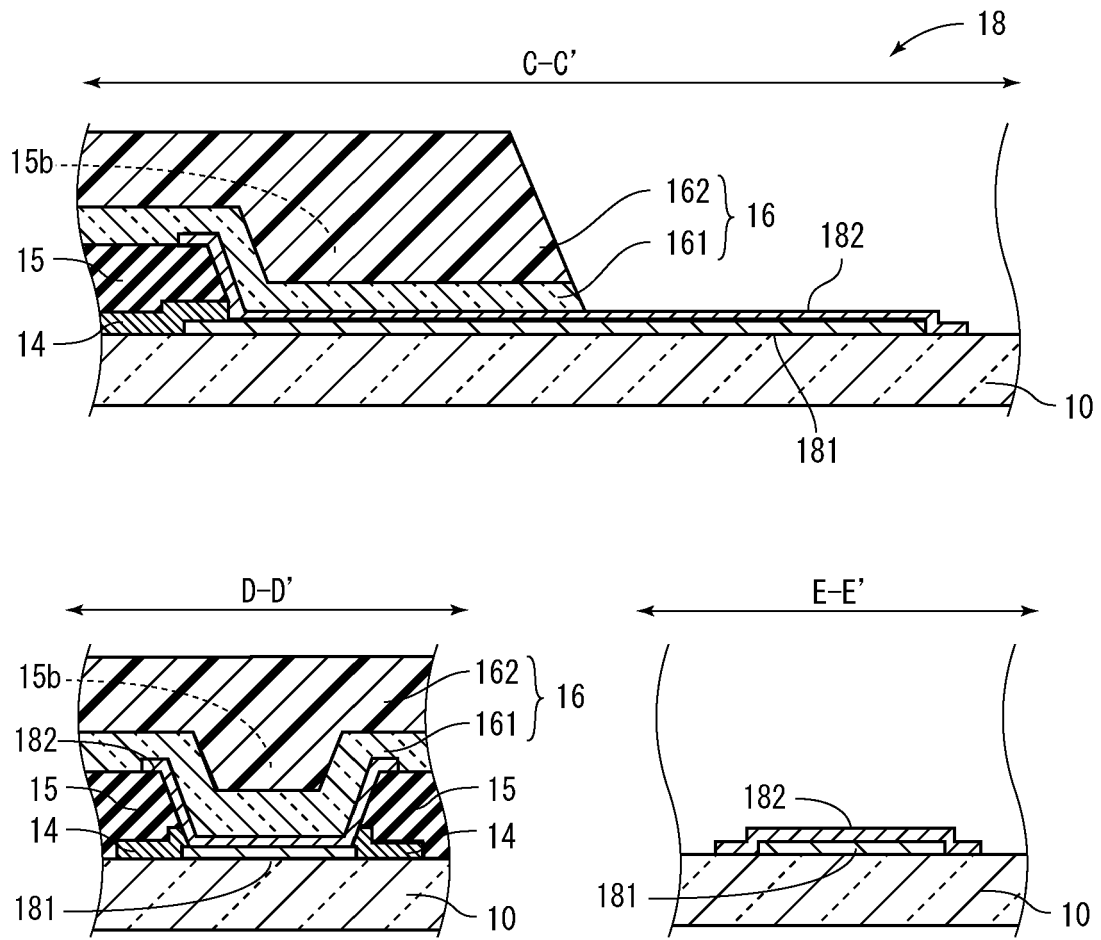
[図3]



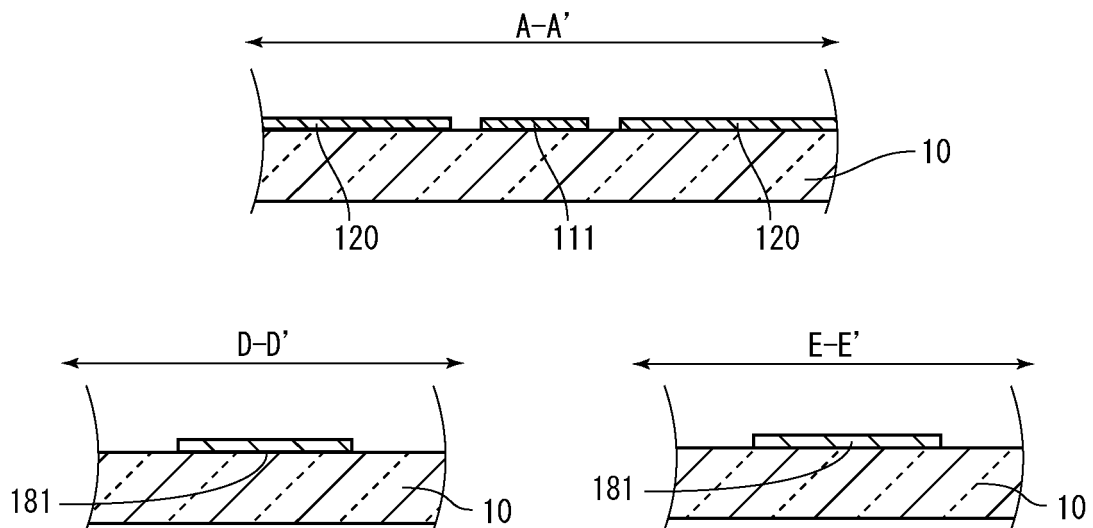
[図4]



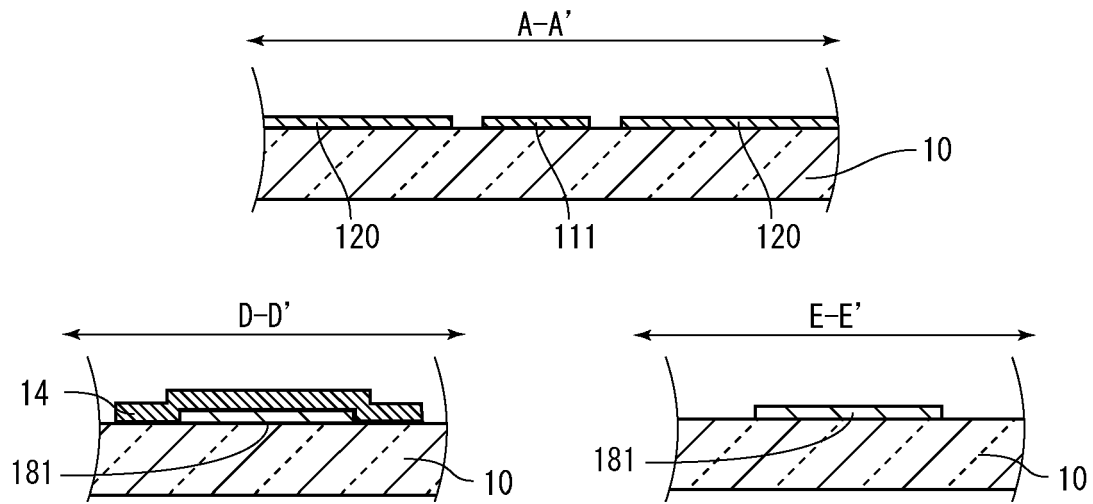
[図5]



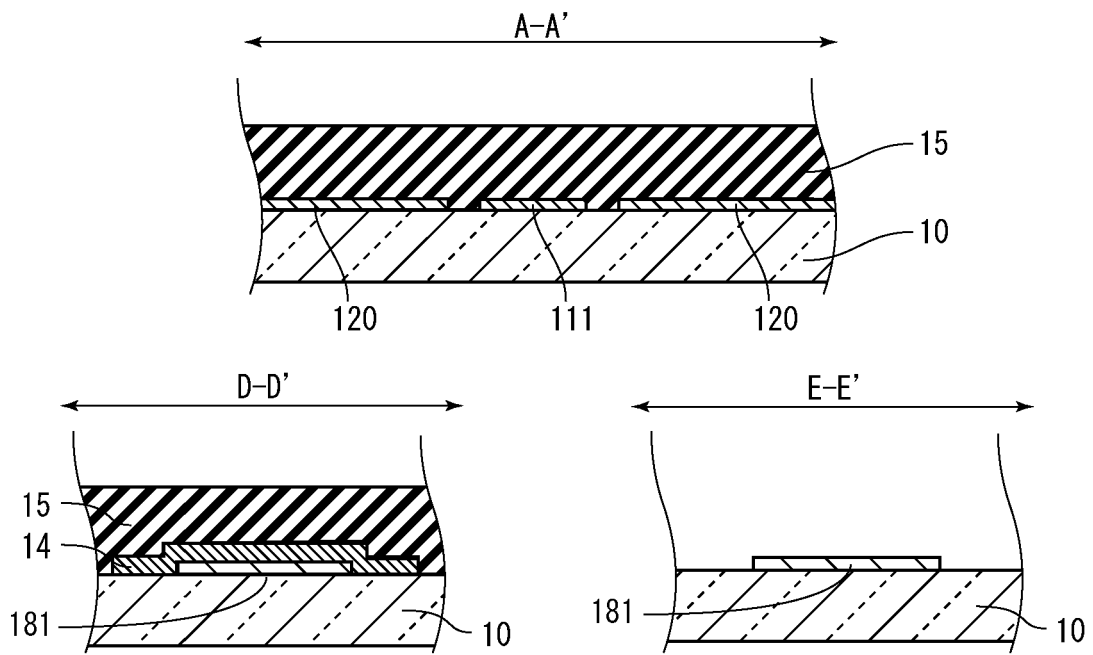
[図6A]



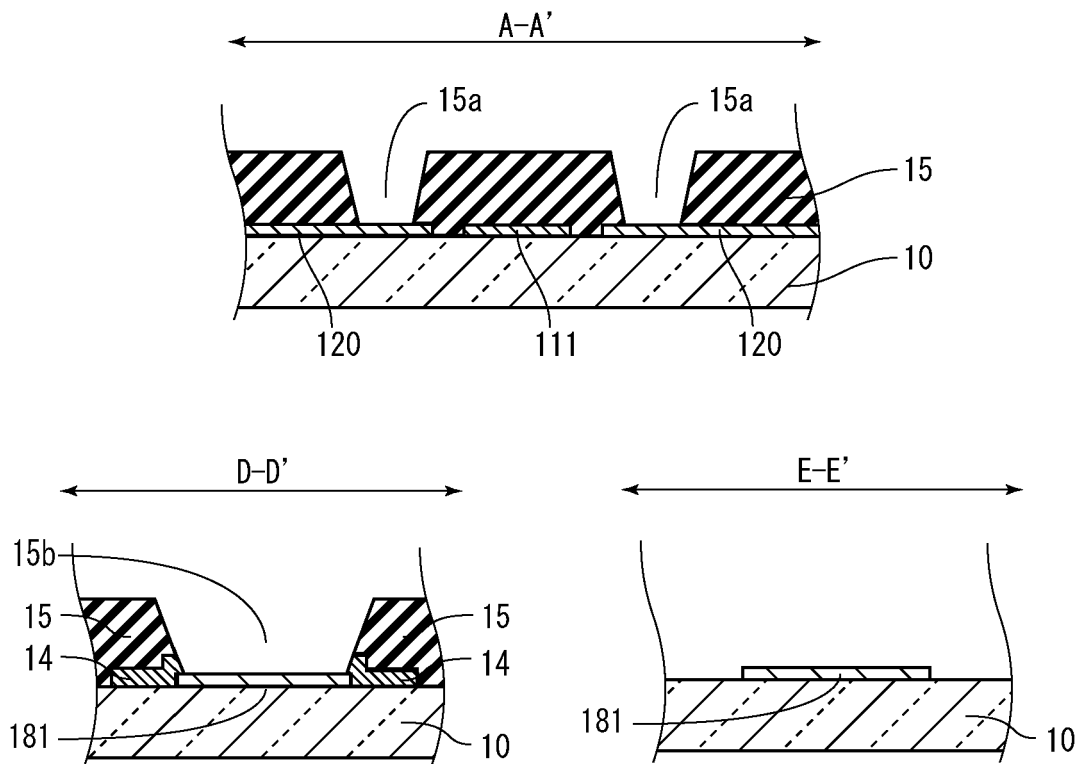
[図6B]



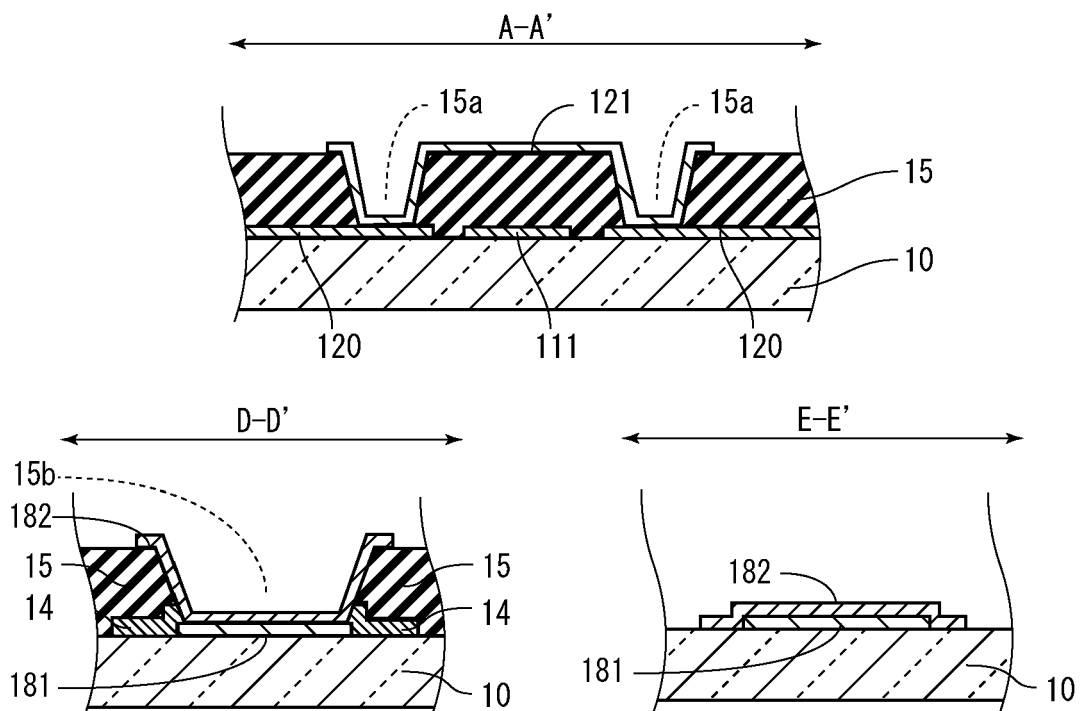
[図6C]



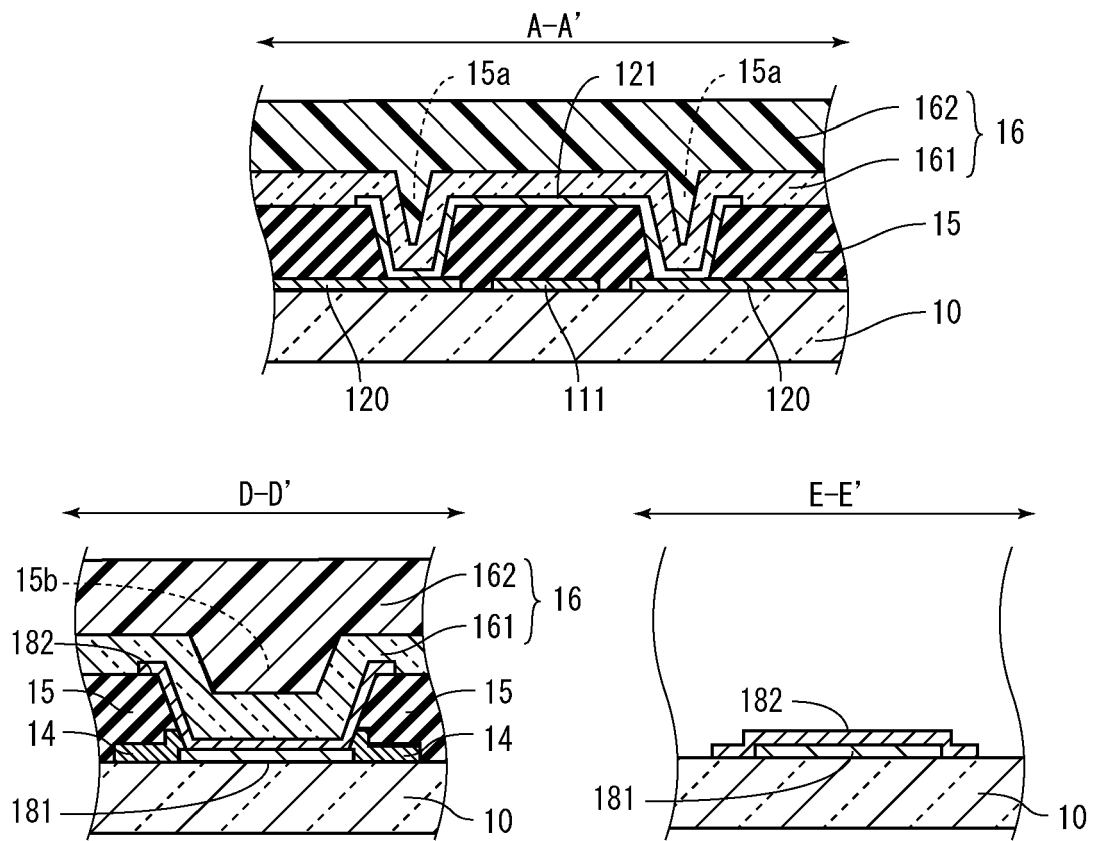
[図6D]



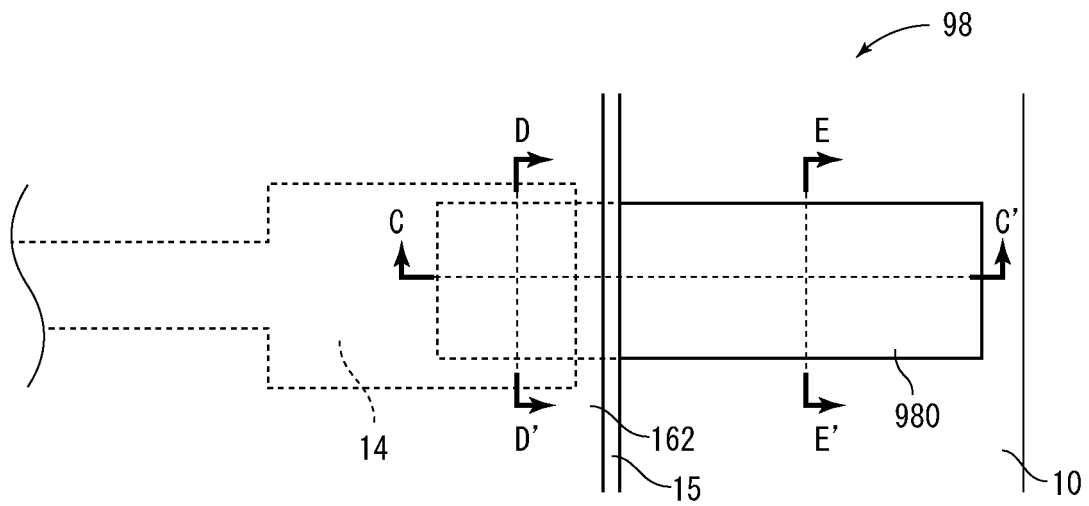
[図6E]



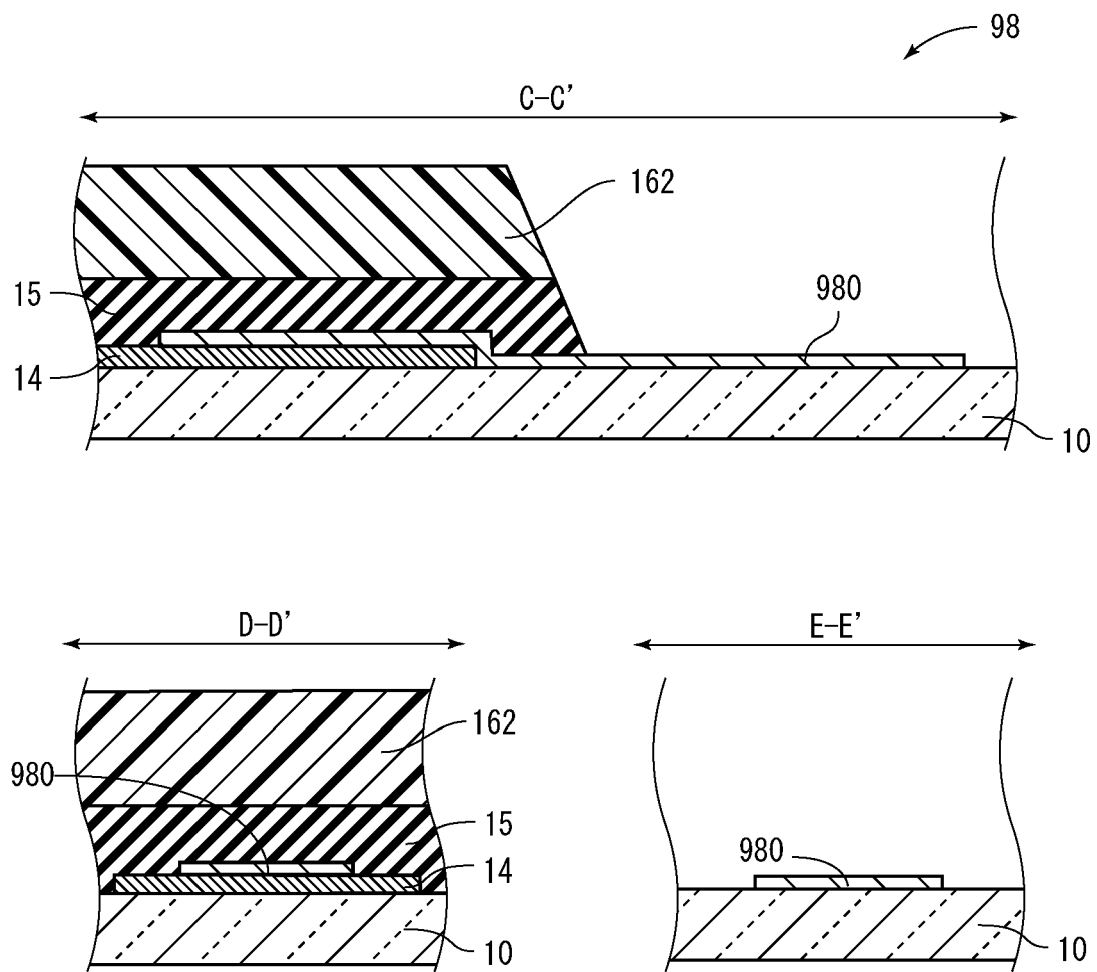
[図6F]



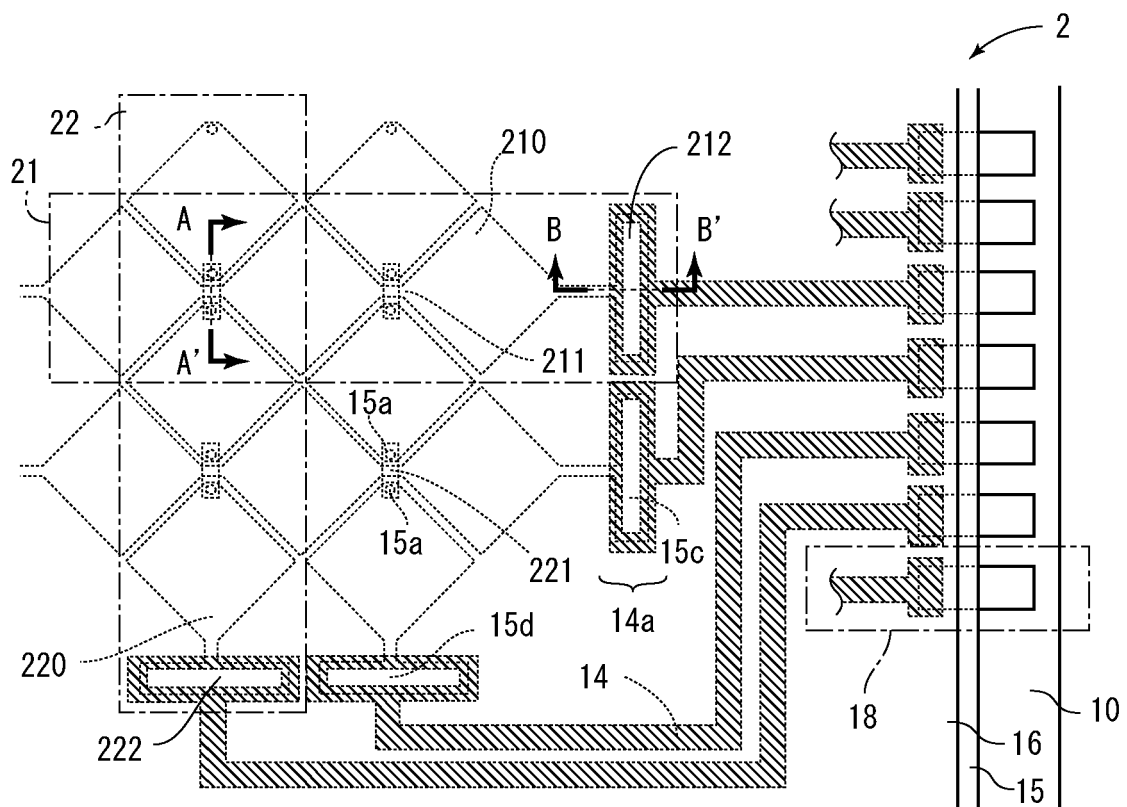
[図7]



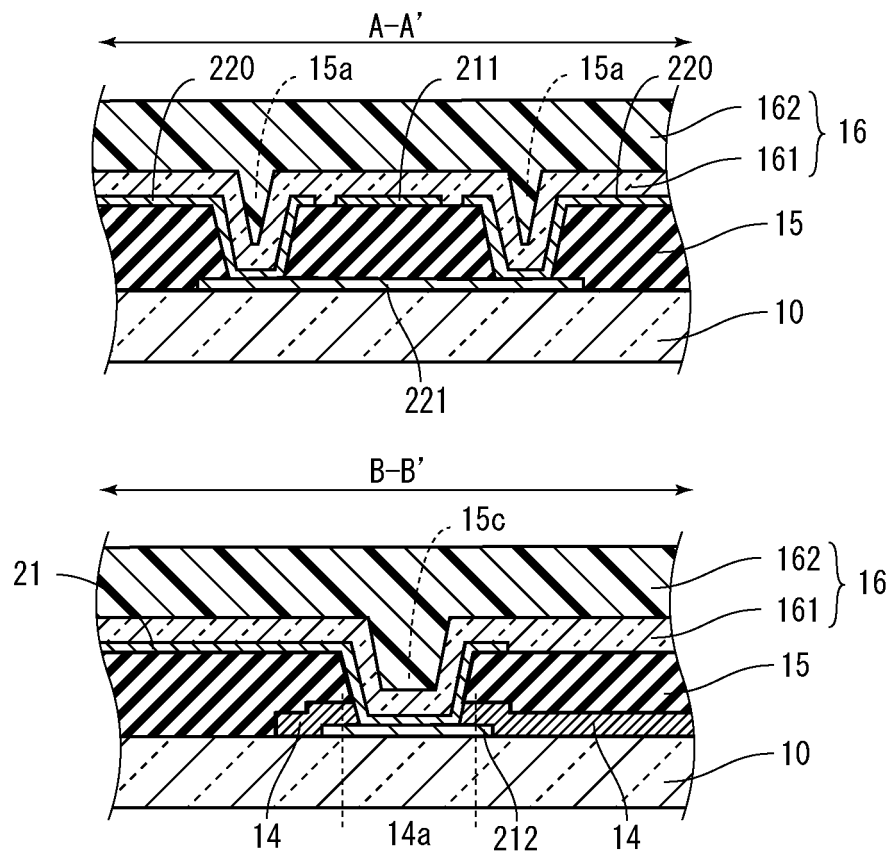
[図8]



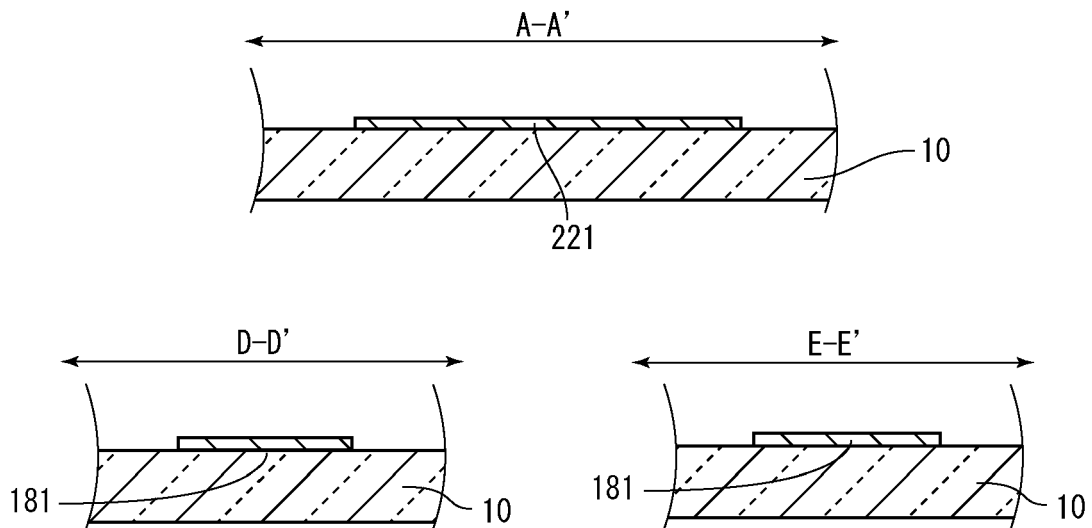
[図9]



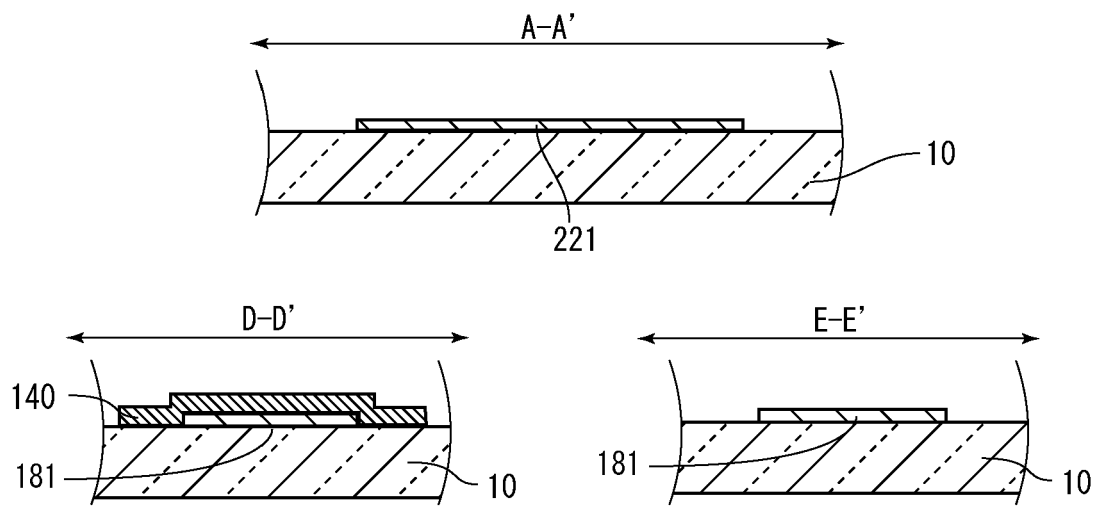
[図10]



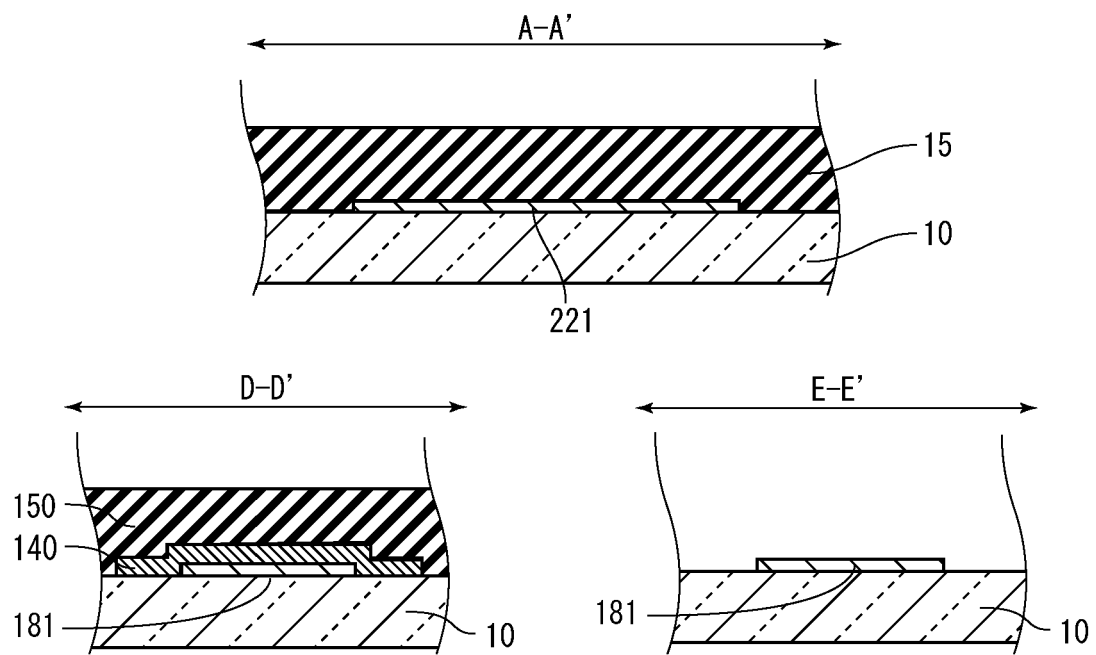
[図11A]



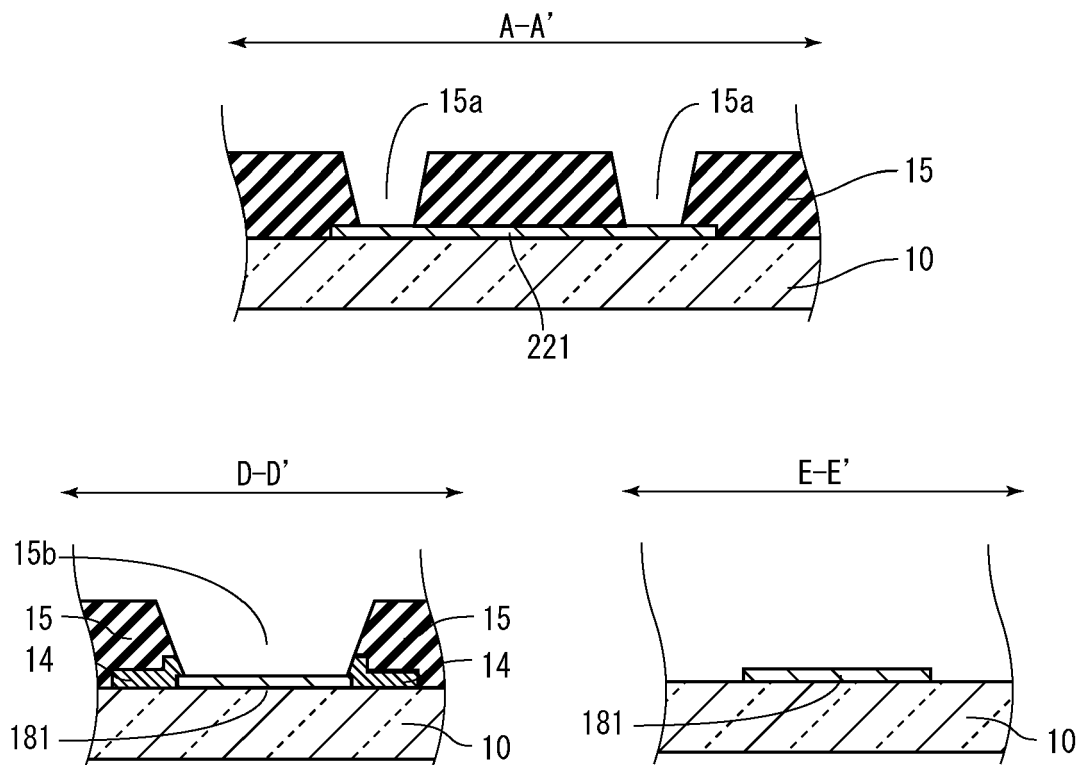
[図11B]



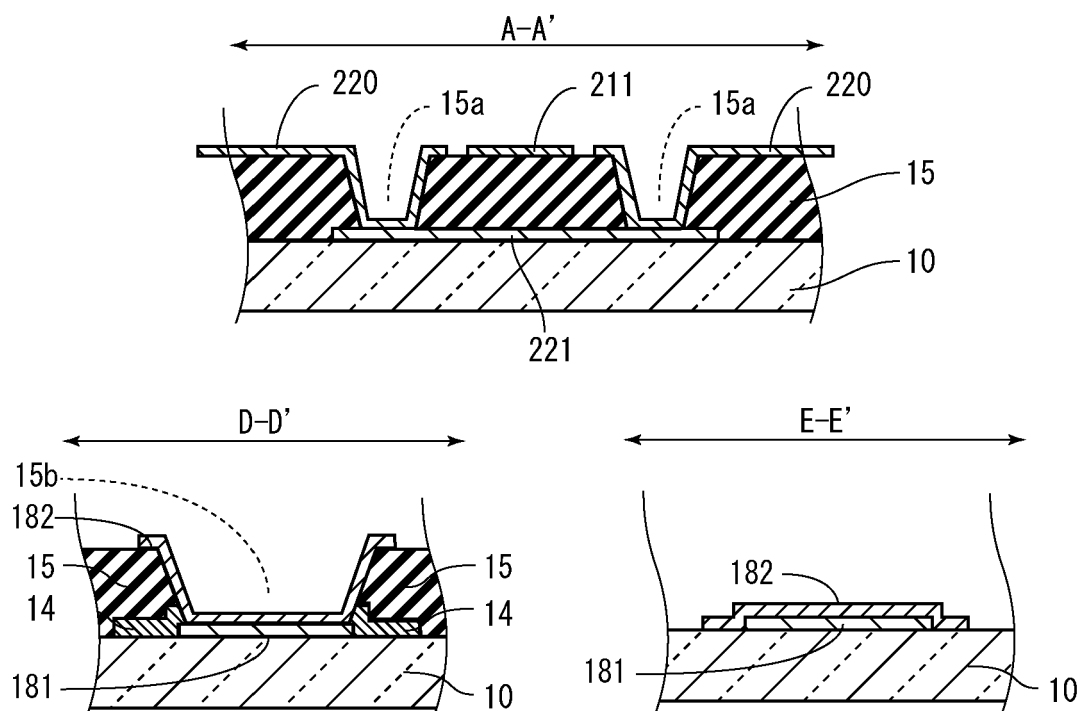
[図11C]



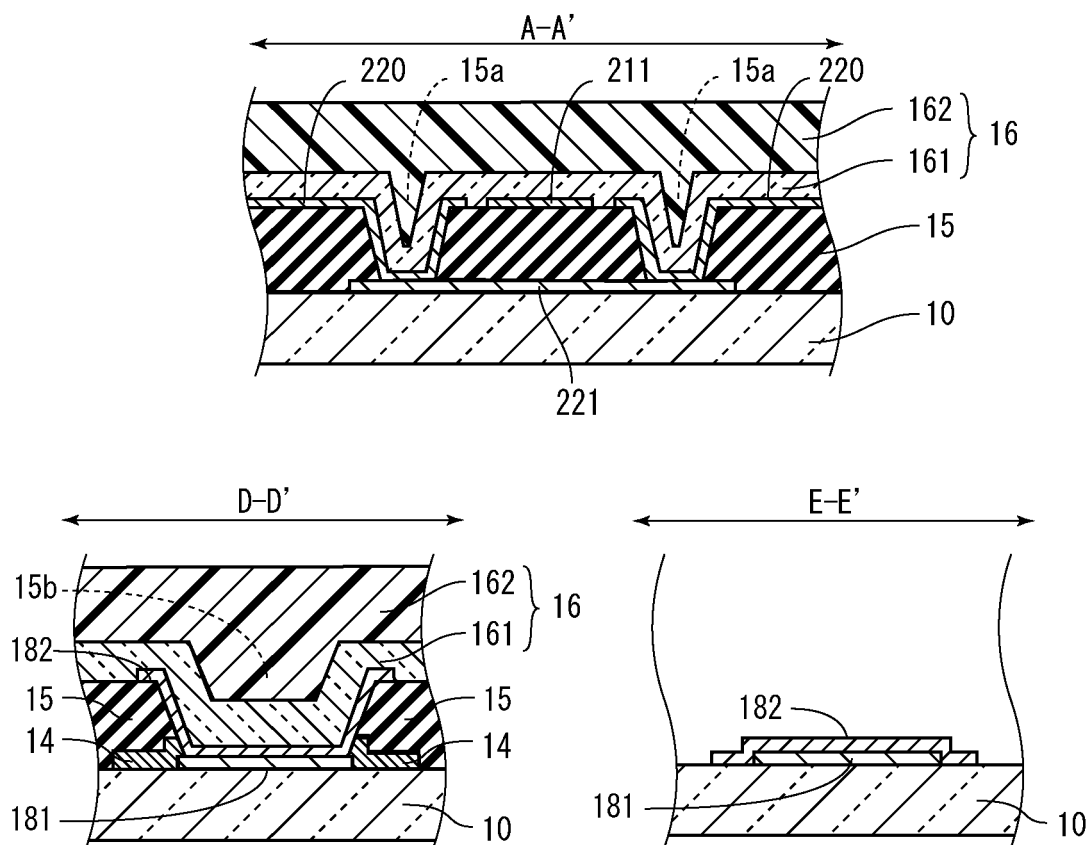
[図11D]



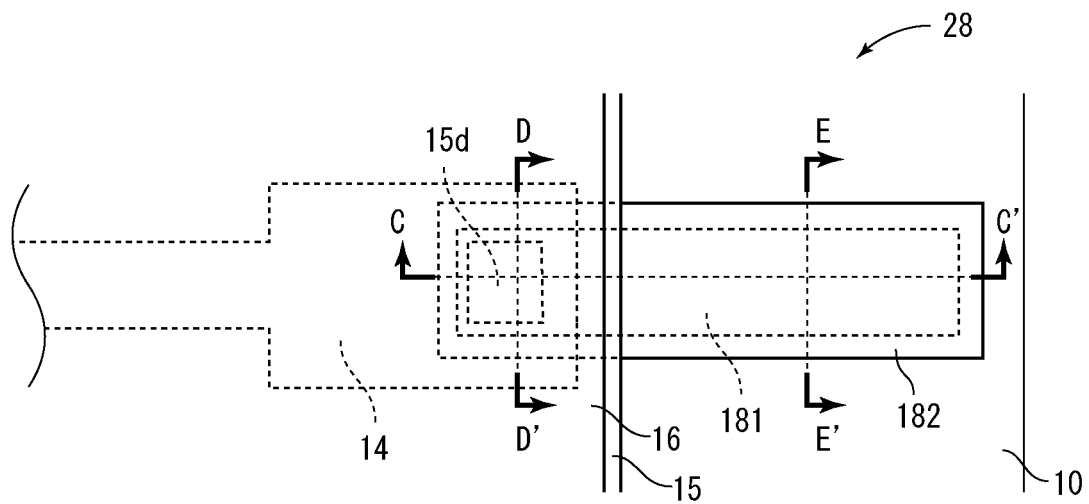
[図11E]



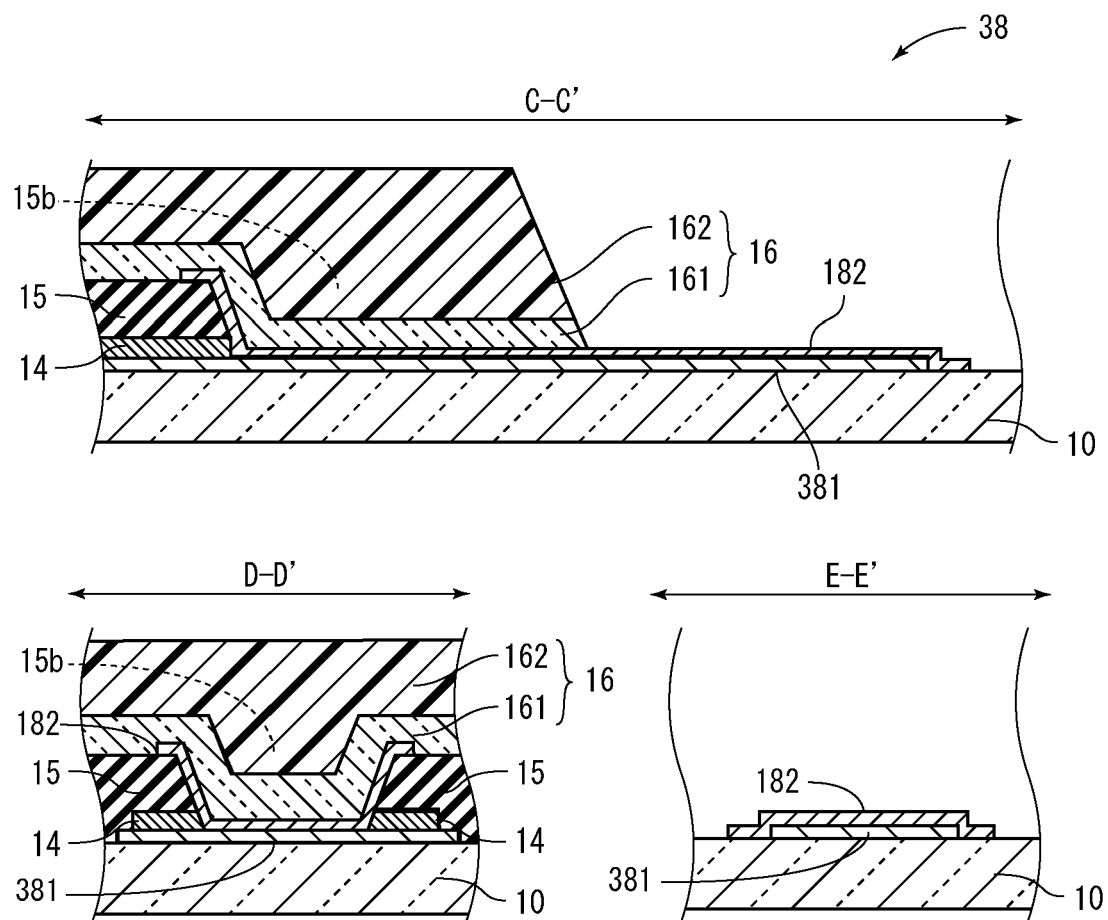
[図11F]



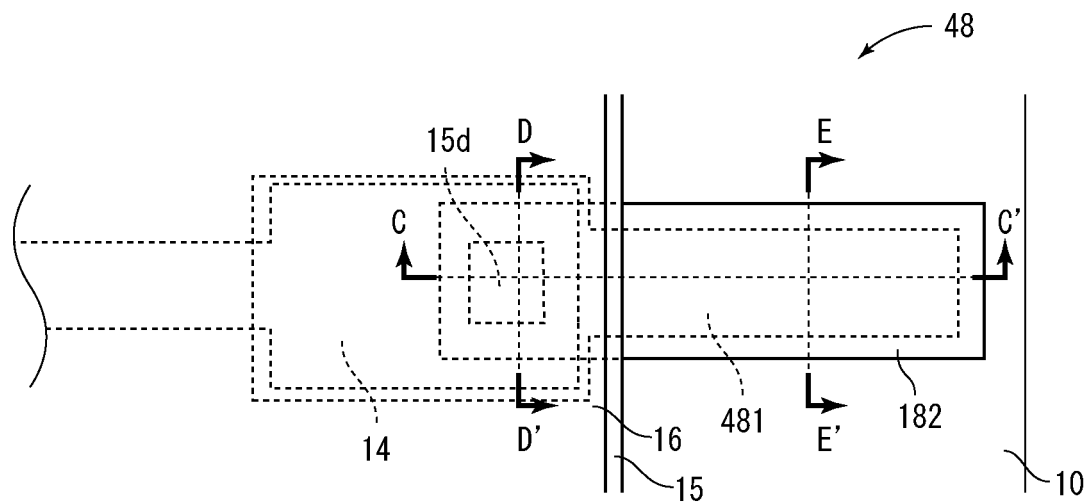
[図12]



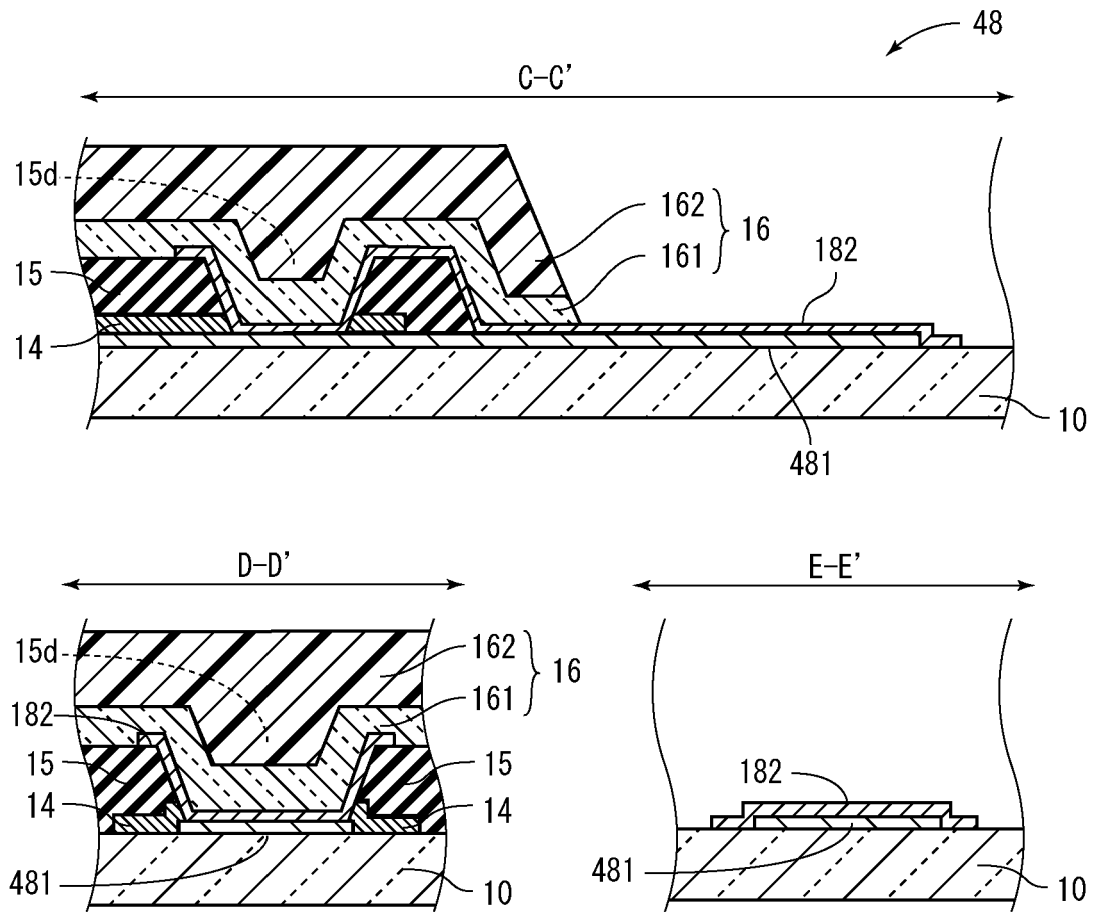
[図15]



[図16]



[図17]



[図18]

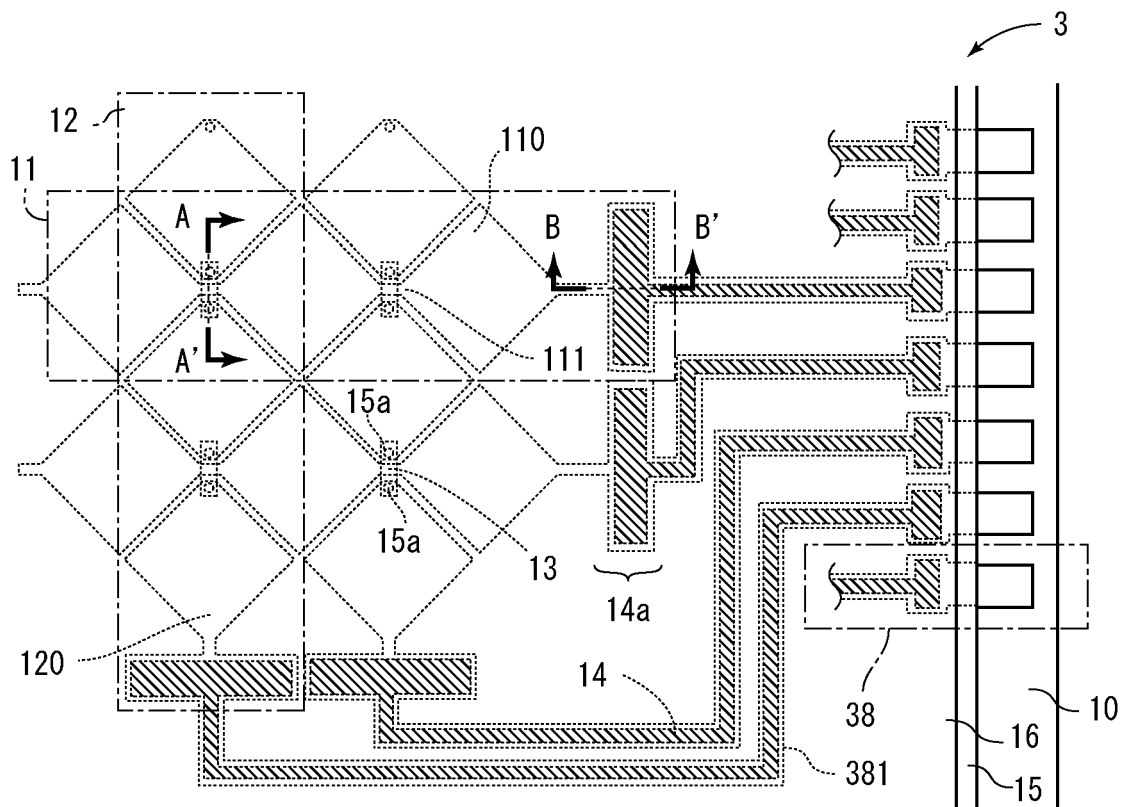
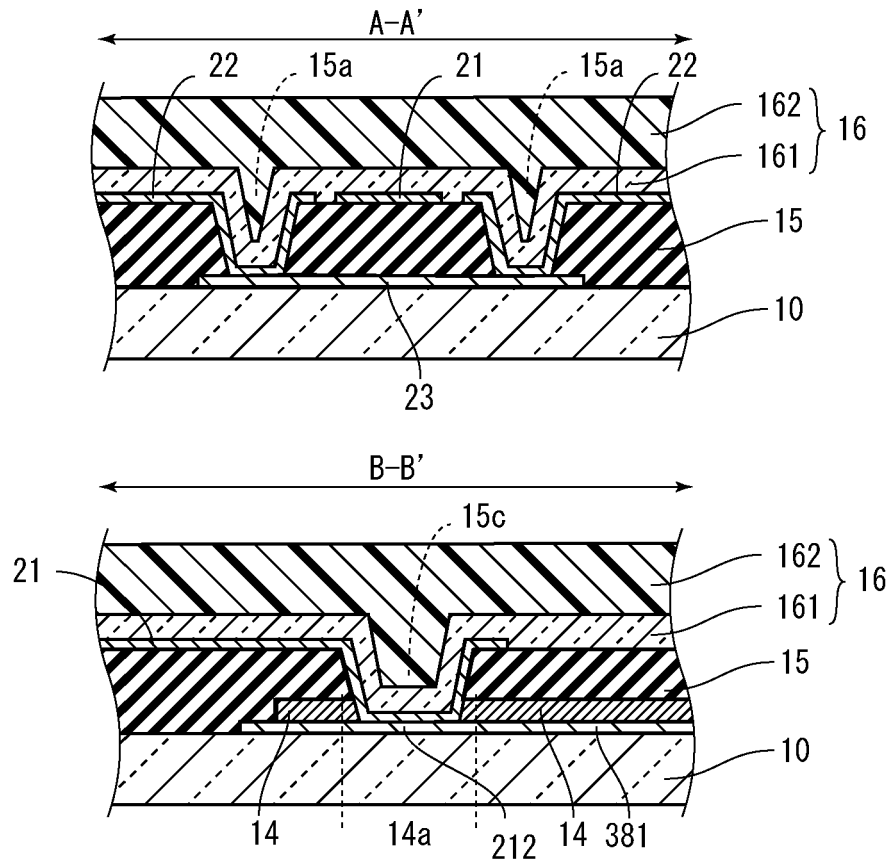


Figure 1 consists of two cross-sectional views, (A) and (B), of a semiconductor device.
 View (A) is labeled A-A' and shows a substrate 10 with a thin layer 11. A patterned layer 12 is formed on top of layer 11. Above layer 12 is a layer 13, followed by a layer 15. The topmost layer is 16, which is composed of sub-layers 161 and 162.
 View (B) is labeled B-B' and shows a substrate 10 with a thin layer 11. A layer 14 is formed on top of layer 11. Above layer 14 is a layer 15, followed by a top layer 16 with sub-layers 161 and 162. A dashed line 381 is shown within the substrate 10.

[図21]



[図22]

