WHAT IS CLAIMED IS:

1. An image processing device for performing a data decompression, the device comprising:

a decoder circuit comprising a plurality of stages for decompressing first compressed image data of a plurality of pixels to original image data, the stages comprises at least first and second stages;

an intellectual property (IP) core;

a memory device;

wherein the decoder circuit is configured to divide the pixels into a plurality of groups comprising at least first and second groups that are adjacent one another,

wherein the first stage performs prediction compensation on the first compressed image data of a first pixel of the first group at a first time to generate first prediction data, and performs the prediction compensation on the first compressed image data of a second pixel of the first group at a second time using the first prediction data, and

wherein the second stage performs the prediction compensation on the first compressed image data of a first pixel of the second group at the second time using the first prediction data, to generate second prediction data

wherein the decoder circuit receives the first compressed image data from the IP core and outputs the original image data to the IP core.

2. The image processing device of claim 1, wherein the performing of the prediction compensation on the first compressed image data of the first pixel comprises adding the first compressed image data of the first pixel to half a bit depth of the original image data to generate the first prediction data.

3. The image processing device of claim 1 or claim 2, wherein the first and second groups are located in a same first row.

4. The image processing device of any one of claims 1 to 3, wherein the decoder circuit comprises a first logic circuit to perform entropy decoding on second compressed image data of the pixels, and the first compressed image data is generated from a result of the entropy decoding.

5. The image processing device of claim 4, wherein the first compressed image data is the result of the entropy decoding when a lossless decompression is selected.

6. The image processing device of claim 4 or claim 5, wherein the decoder circuit comprises a second logic circuit to perform inverse quantization on result of the entropy decoding and the first compressed image data is a result of the inverse quantization when a lossy decompression is selected.

7. The image processing device of any one of claims 1 to 6, wherein the decoder circuit comprises a lossy decompression path and a lossless decompression path, and the encoder circuit further comprises a mode selection circuit configured to enable one of the lossy decompression path and lossless decompression path in response to receipt of a control signal.

8. The image processing device of any one of claims 3 to 7, wherein the groups comprise a third group in a second row adjacent the first row, wherein the decoder circuit performs the prediction compensation on the first compressed image data of a first pixel of the third group using the first prediction data.

9. The image processing device of claim 8, wherein the groups comprise a fourth group adjacent the third group in the second row, wherein the decoder circuit performs the prediction compensation on the first compressed image data of a first pixel of the fourth group using the second prediction data.

10. The image processing device of any one of claims 1 to 9, further comprising:
a databus connected to the IP core and the memory device,
wherein the IP core is connected to the decoder circuit; and
wherein the IP core forwards the original image data across the databus for storage in the memory device.

11. The image processing device of any one of claims 1 to 9, further comprising:
a databus connected to the IP core, the memory device, and the decoder circuit,
wherein the IP core transmits the first compressed image data to the decoder circuit using the databus, and

wherein the decoder circuit outputs the original image data across the databus for storage in the memory device.

12. The image processing device of any one of claims 1 to 9, further comprising:

a databus connected to the IP core and the decoding circuit,

wherein the memory device is connected to the decoder circuit,

wherein the IP core transmits the first compressed image data to the decoder circuit using the databus, and

wherein the decoder circuit stores the original image data in the memory device.

13. An image processing device for performing a data compression, the device comprising:

an encoder circuit comprising a plurality of stages for compressing original image data of a plurality of pixels to first compressed image data, the stages comprises at least first and second stages;

an intellectual property (IP) core;

a memory device,

wherein the encoder circuit is configured to divide the pixels into a plurality of groups comprising at least first and second groups that are adjacent one another,

wherein the first stage processes the original image data of a first pixel of the first group at a first time to generate first prediction data, processes the original image data of a second pixel of the first group and the first prediction data at a second time to generate first residual data,

wherein the second stage processes the original image data of a first pixel of the second group and the first prediction data at the second time to generate to generate second residual data,

wherein the first compressed image data includes the first prediction data, the first residual data, and the second residual data

wherein the encoder circuit receives the original image data from the IP core and outputs the first compressed image data to the IP core, and

wherein the IP core forwards the first compressed image data.

14. The image processing device of claim 13, wherein the first residual data is a difference between the first prediction data and the original image data of the first pixel of the first group, and the second residual data is a difference between the first prediction data and the original image data of the first pixel of the second group.

15. The image processing device of claim 13 or claim 14, wherein the first and second groups are located in a same first row.

16. The image processing device of any one of claims 13 to 15, wherein the encoder circuit performs entropy encoding on the first compressed image data to generate second compressed image data when a lossless compression is selected.

17. The image processing device of any one of claims 13 to 16, wherein the encoder circuit performs a quantization on the first compressed image data using a preset quantization parameter (QP) to generate second compressed data, and performs entropy encoding on the second compressed image data to generate third compressed image data when a lossy compression is selected.

18. The image processing device of any one of claims 13 to 17, wherein the encoder circuit comprises a lossy compression path and a lossless compression path, and the encoder circuit further comprises a mode selection circuit configured to enable one of the lossy compression path and lossless compression path in response to receipt of a control signal.

19. The image processing device of any one of claims 13 to 18, wherein the groups comprise a third group in a second row adjacent the first row, wherein the encoder circuit processes the original image data of a first pixel of the third group and the first prediction data to generate third residual data, and the first compressed image data includes the third residual data.

20. The image processing device of any one of claims 13 to 19, further comprising:

a databus connected to the IP core and the memory device,

wherein the intellectual property (IP) core is connected to the encoder circuit; and

wherein the IP core forwards the first compressed image data across the databus for storage in the memory device.