

ABSTRACT

Provided are an apparatus, a memory device, and a method for multi-phase clock training. The memory device includes a clock training circuit configured to receive a clock through a first signal pin, among a plurality of signal pins and connected to a first signal line connected to the first signal pin. The clock training circuit generates a multi-phase clock upon receiving the clock, and generates a three-dimensional (3-D) duty offset code (DOC) for the multi-phase clock by simultaneously phase-sweeping between three internal clock signals in a duty adjustment step in the multi-phase clock. The memory device corrects a duty error of the multi-phase clock using the 3-D DOC.

FIG. 3A