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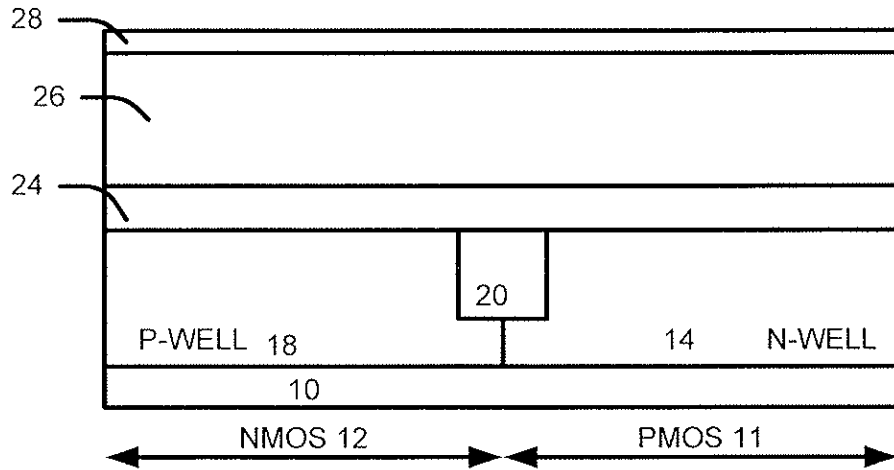


FIGURE 1

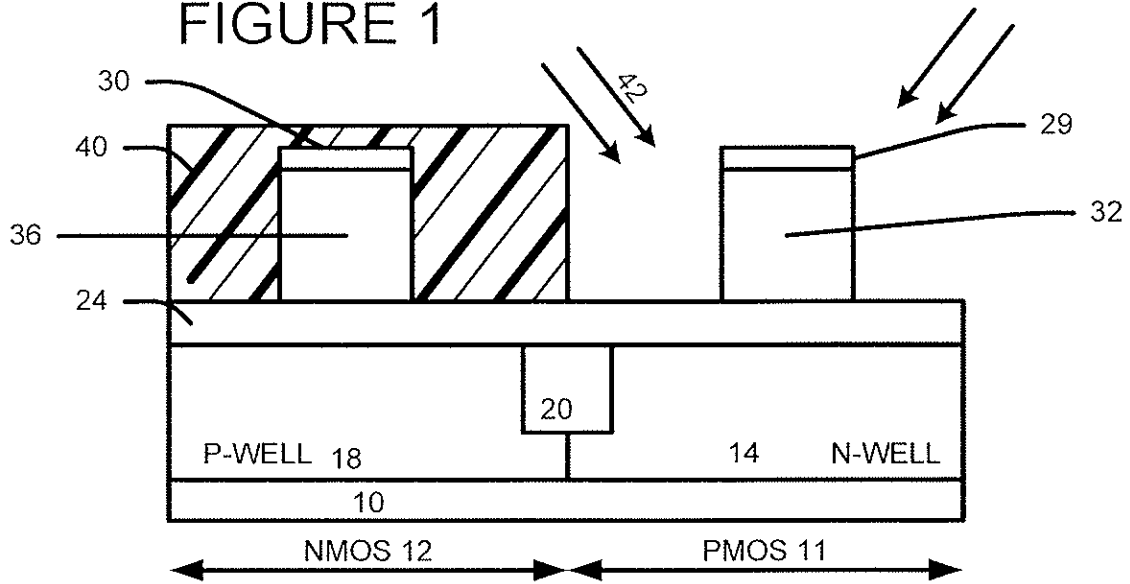


FIGURE 2

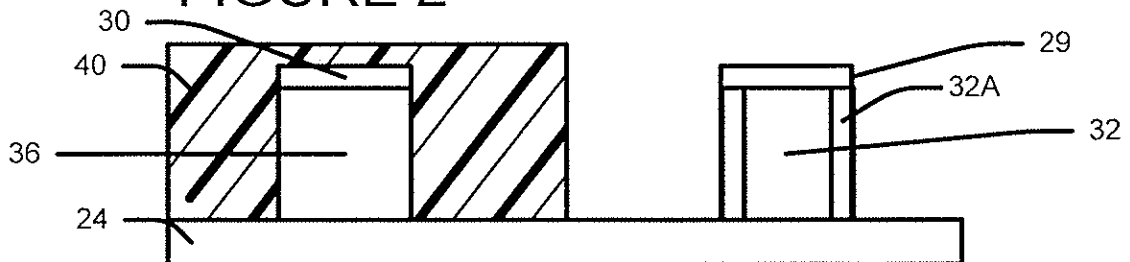


FIGURE 2A

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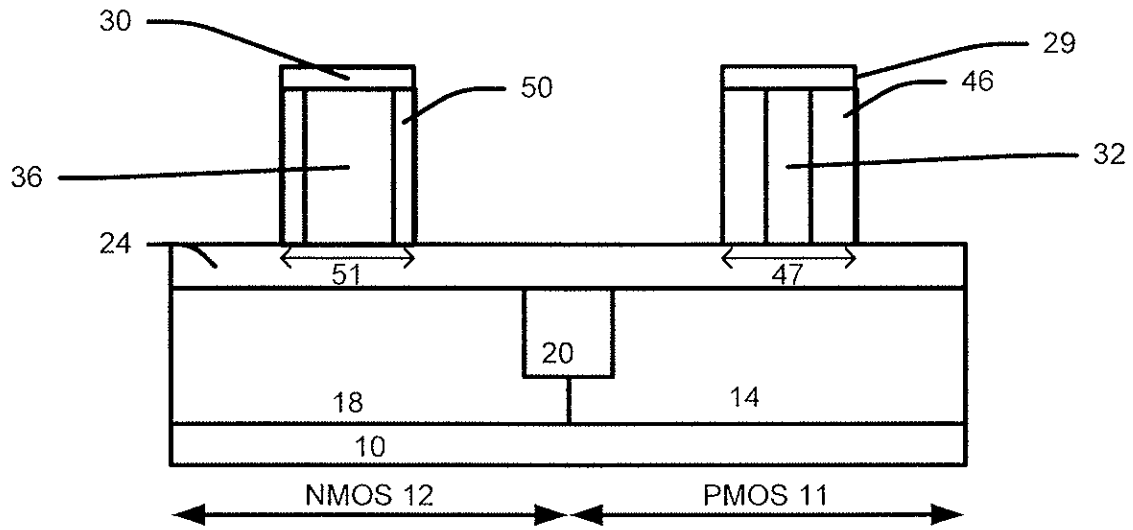


FIGURE 3

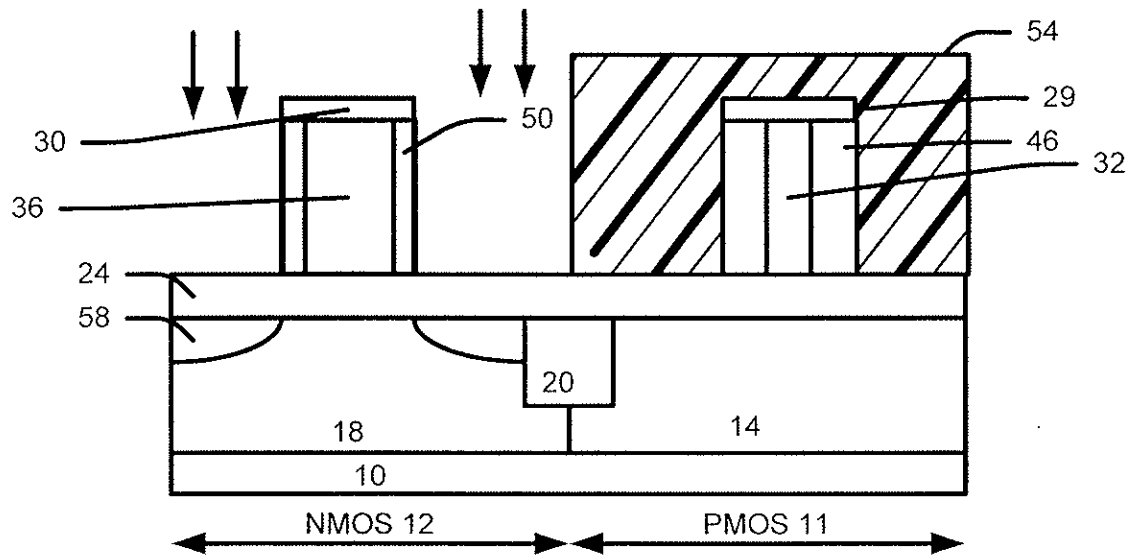


FIGURE 4

A cross-sectional view of a semiconductor device 100. The device consists of a substrate 10 with a central well region 14. On the left side is an NMOS region 12, and on the right side is a PMOS region 11. A gate stack 20 is located in the center of the well region 14. The device is covered by a top layer 30. The NMOS region 12 has a gate stack 36. The PMOS region 11 has a gate stack 29. The well region 14 is defined by a layer 18. The substrate 10 is divided into regions 24 and 58. The well region 14 is defined by a layer 66.

FIGURE 6

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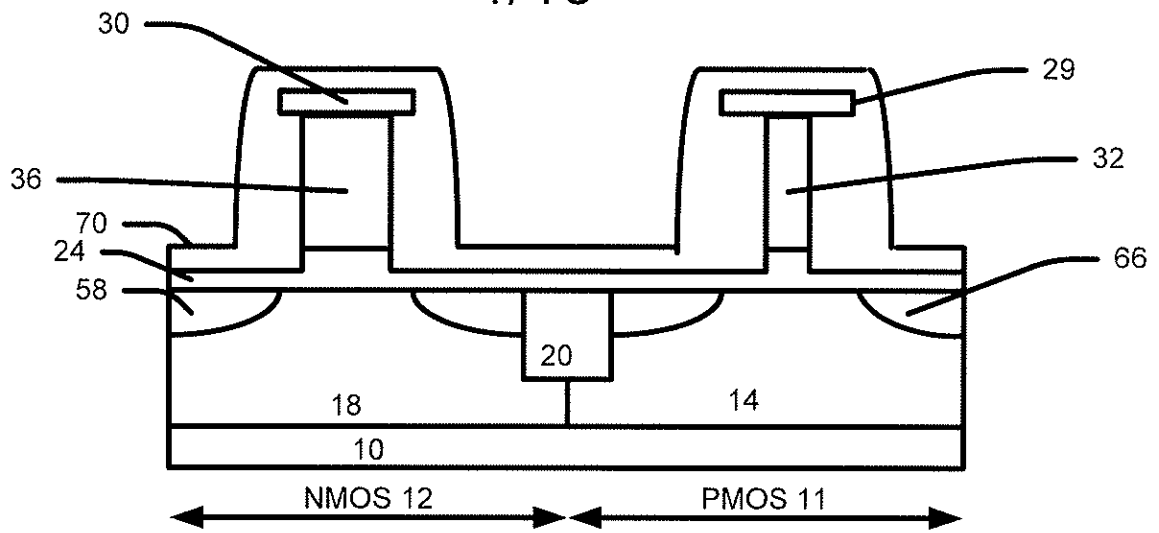


FIGURE 7

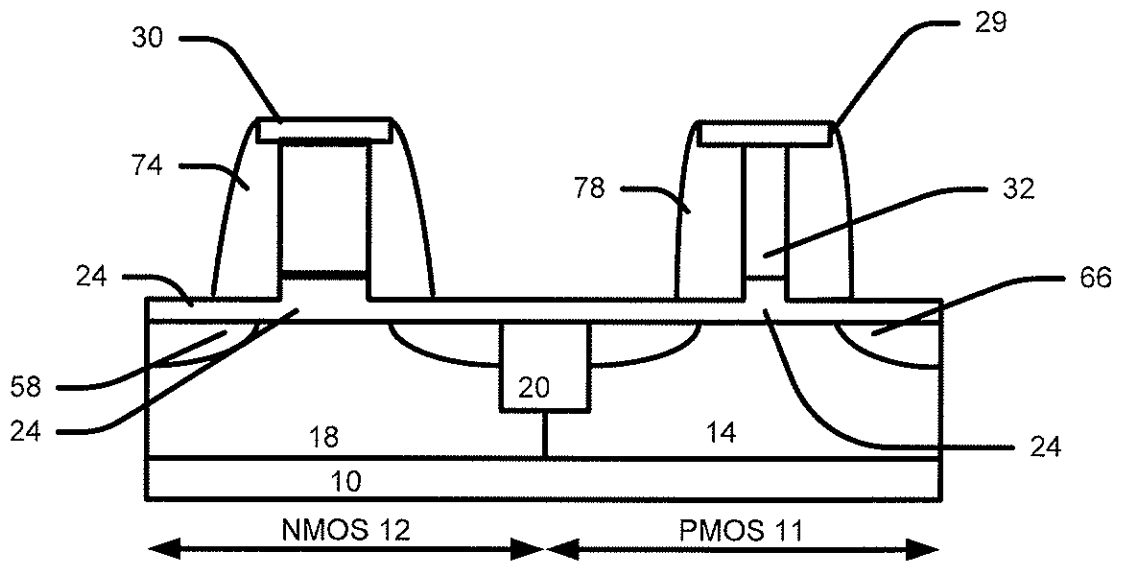
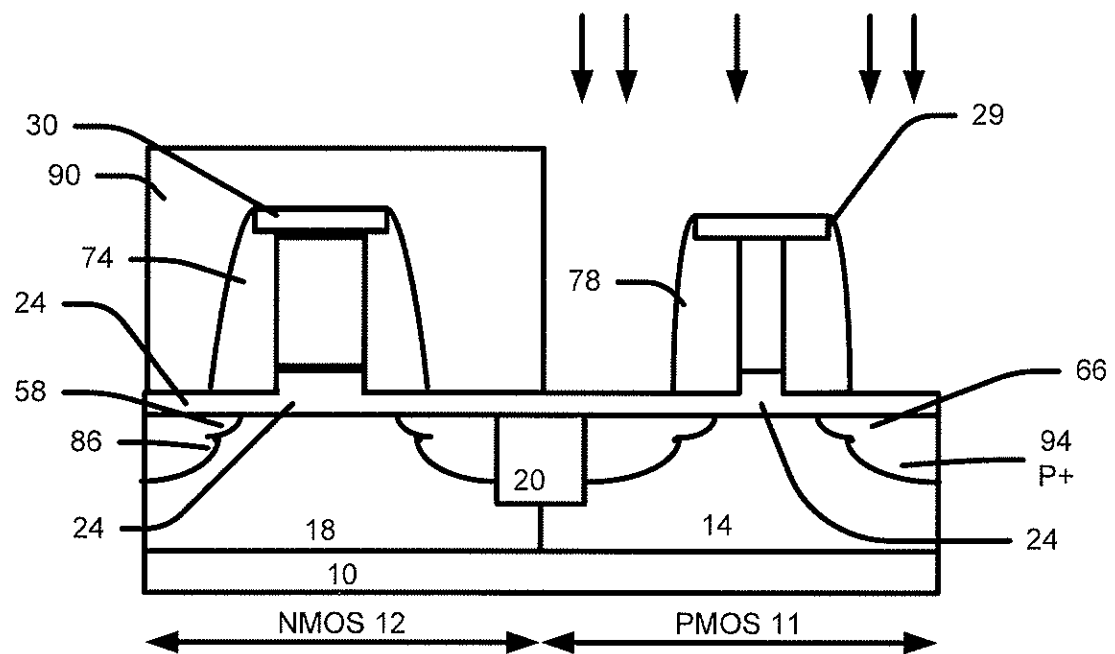
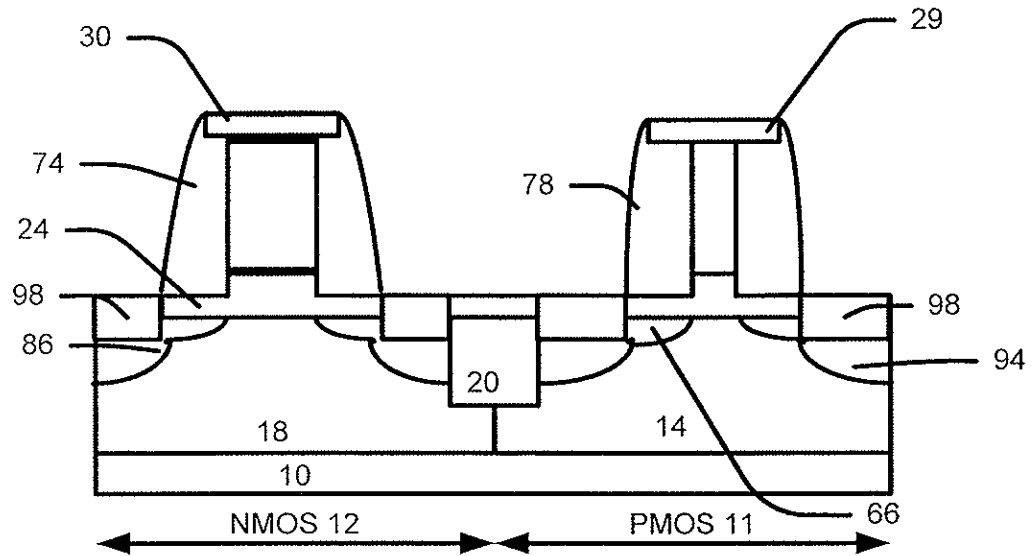


FIGURE 8





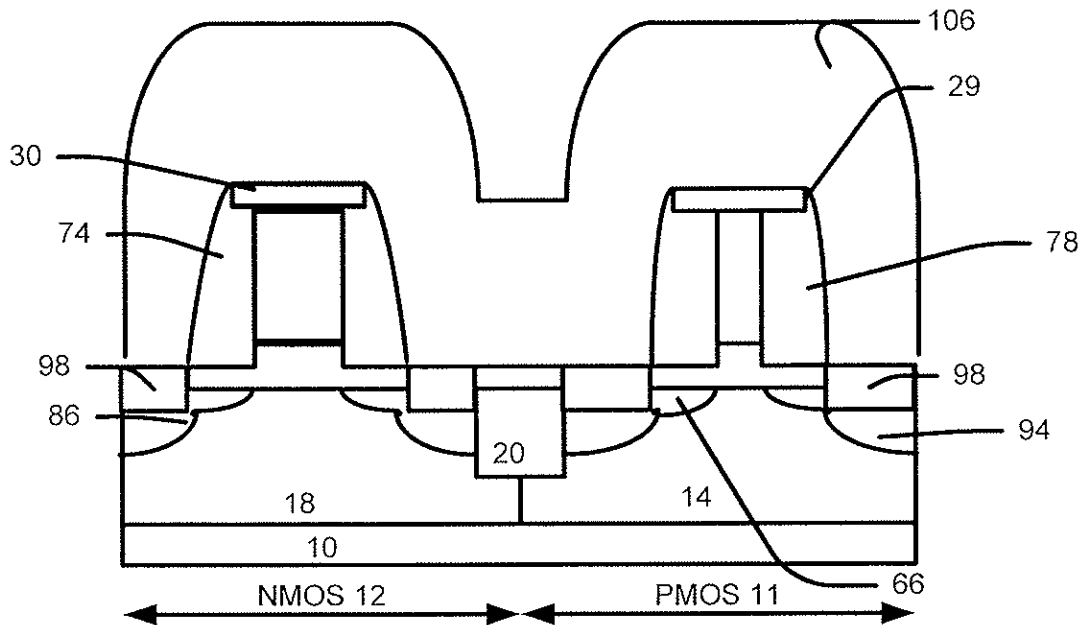


FIGURE 13

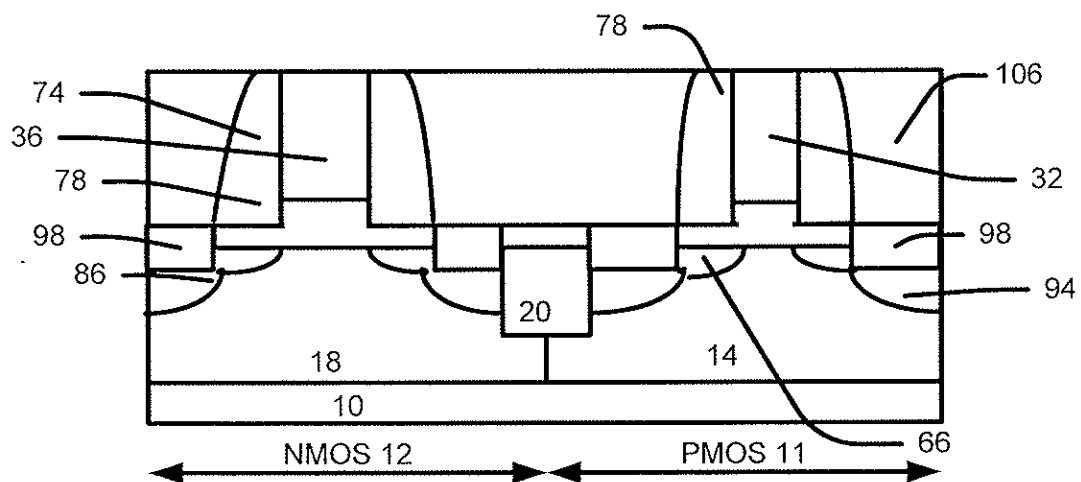


FIGURE 14

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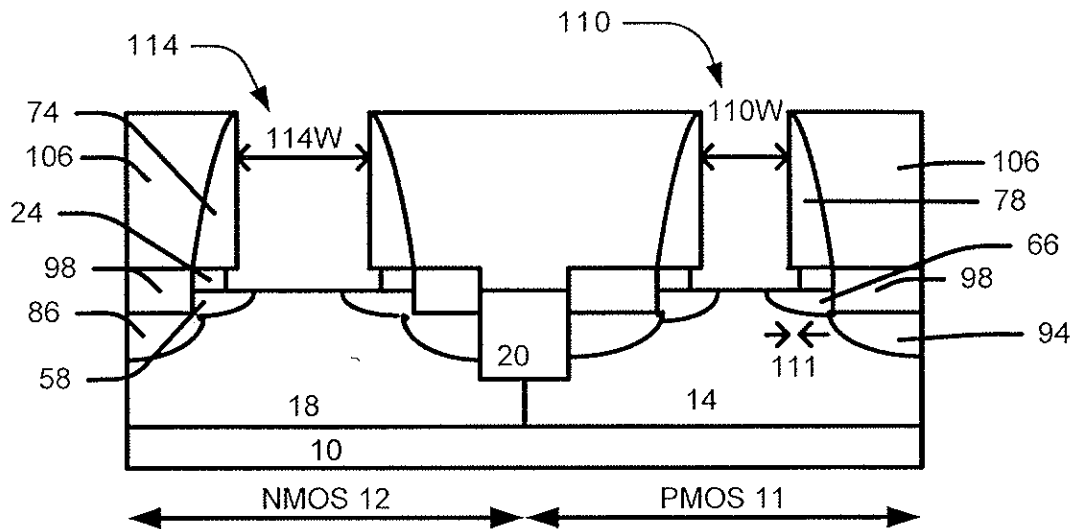


FIGURE 15

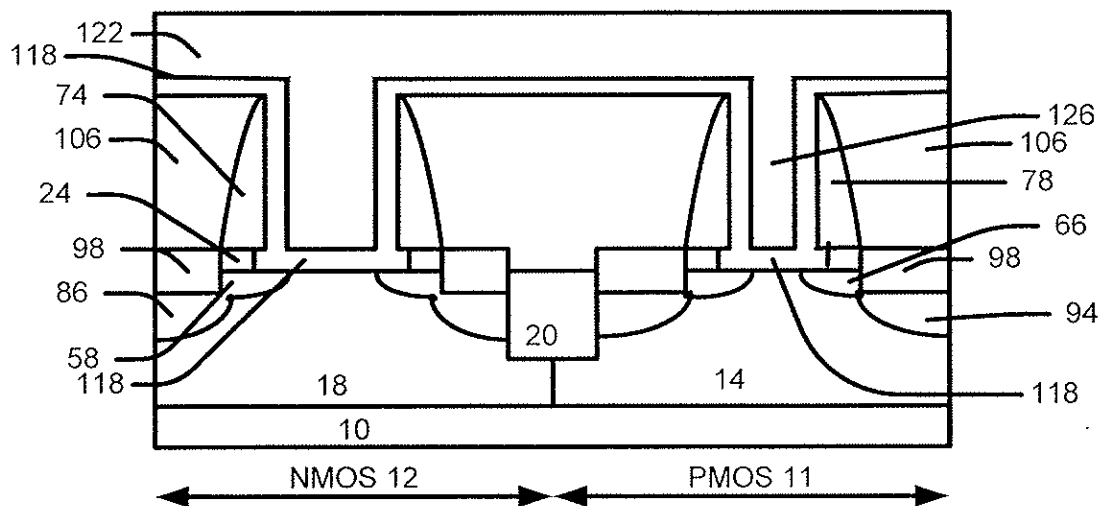


FIGURE 16

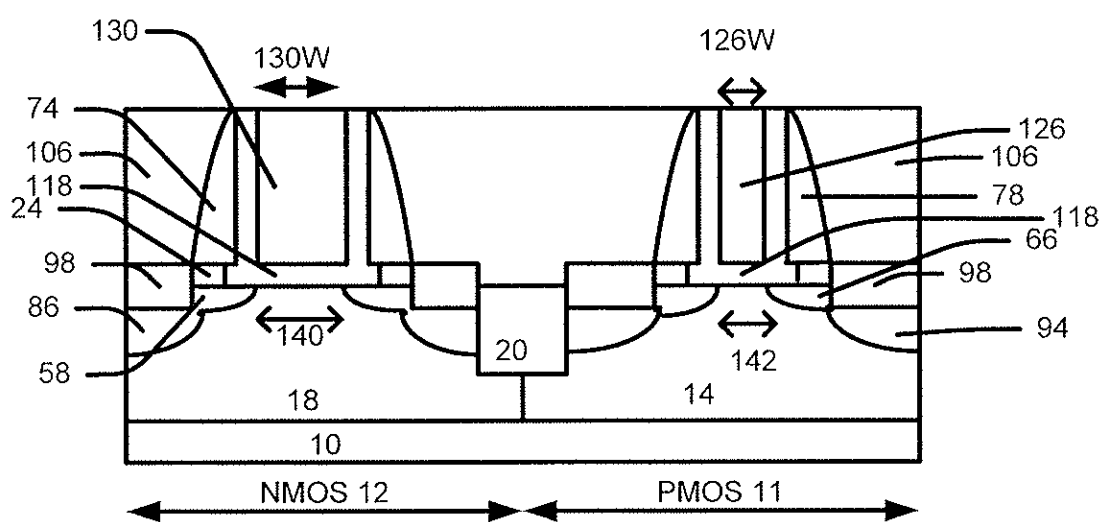


FIGURE 17

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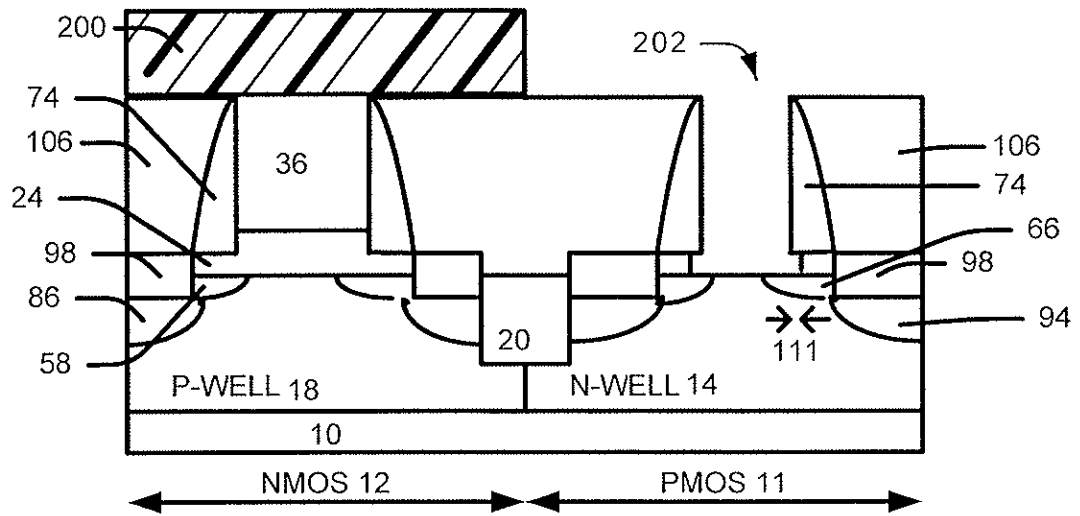


FIGURE 18

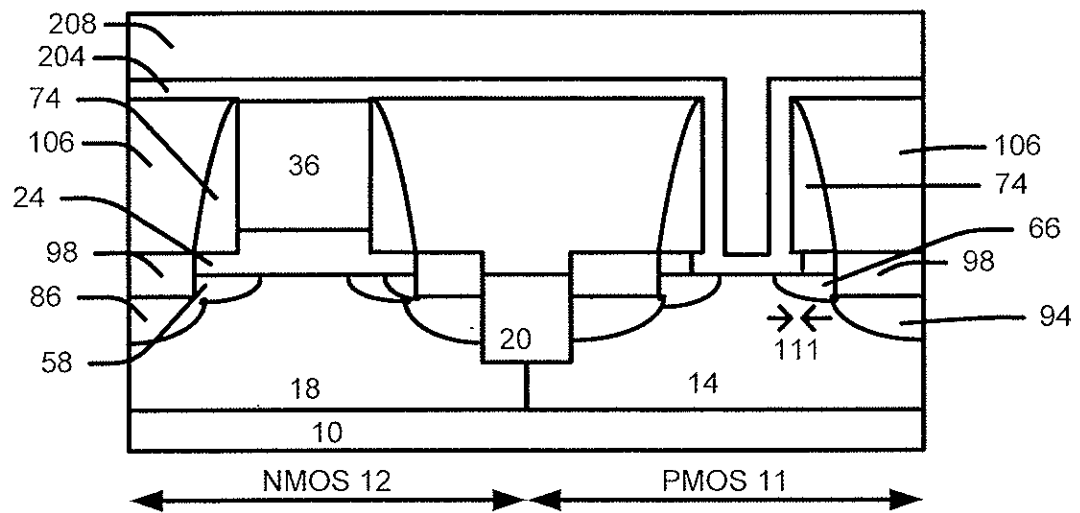


FIGURE 19

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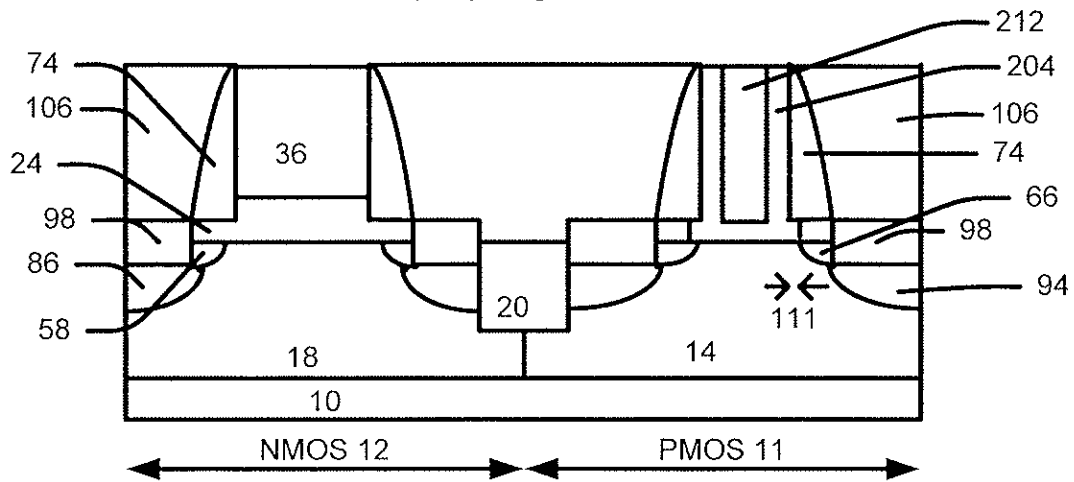


FIGURE 20

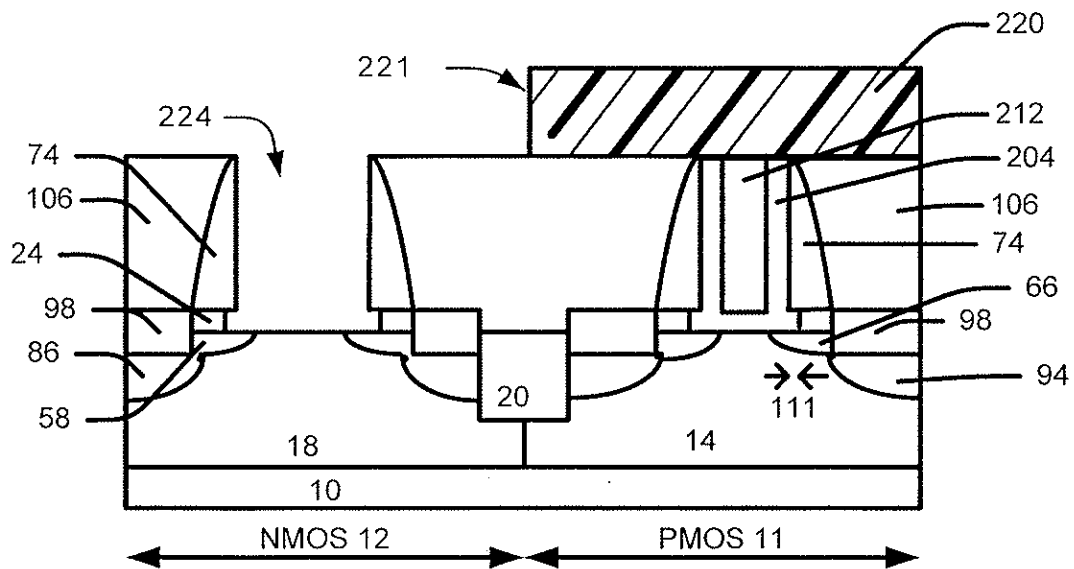


FIGURE 21

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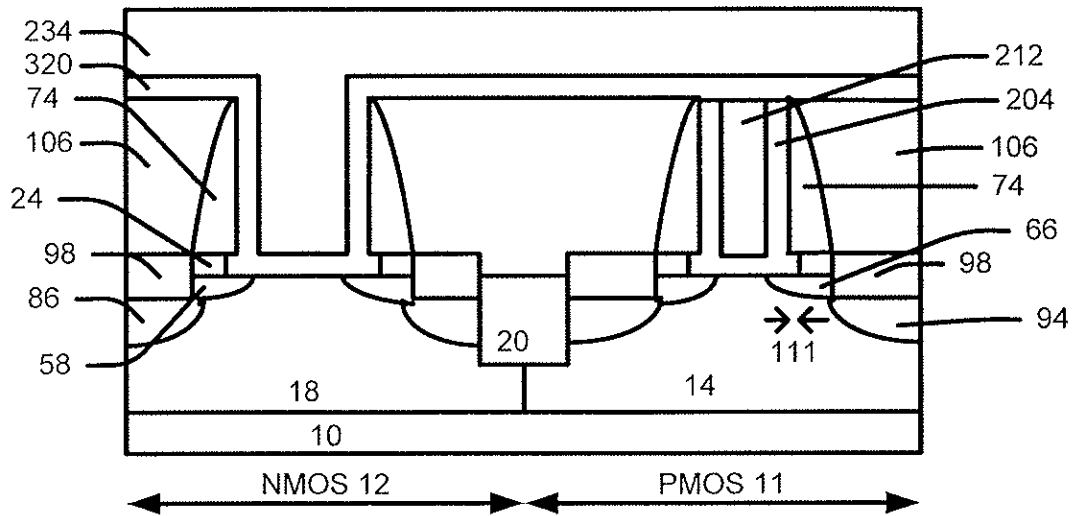


FIGURE 22

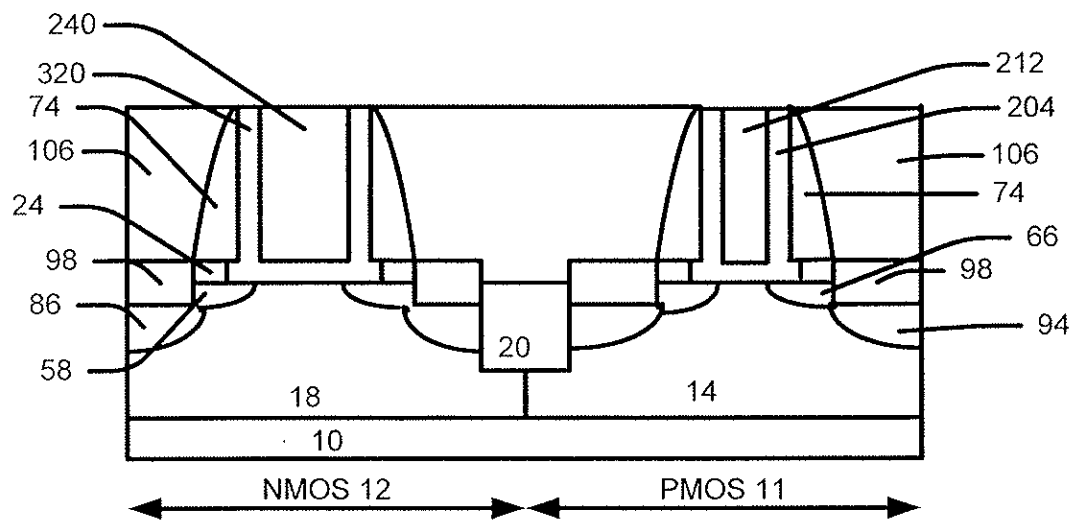


FIGURE 23

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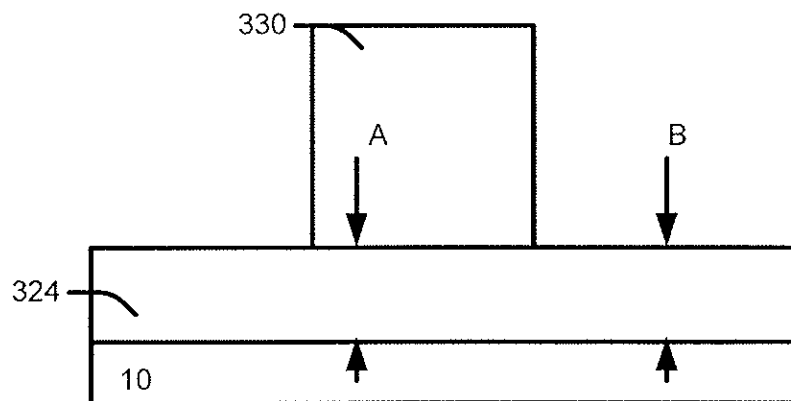


FIGURE 24A

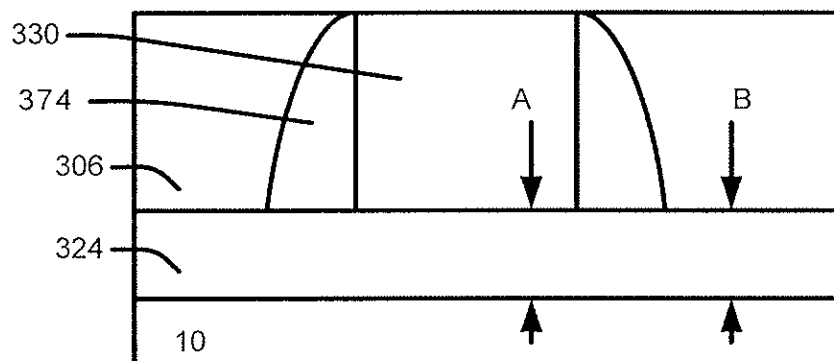


FIGURE 24B

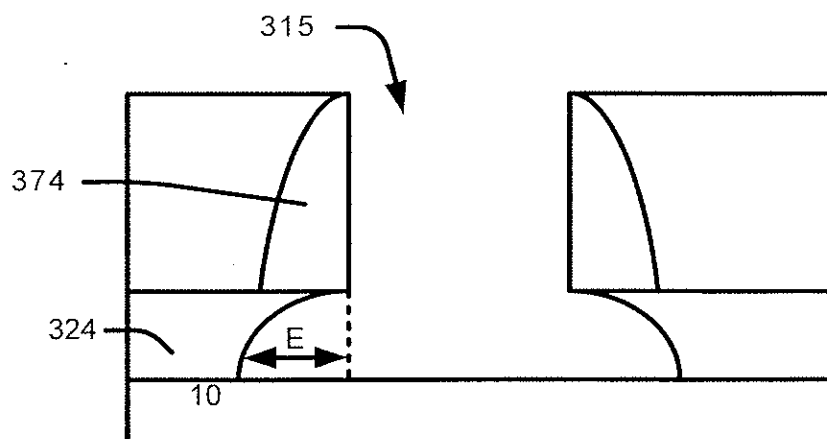


FIGURE 24C

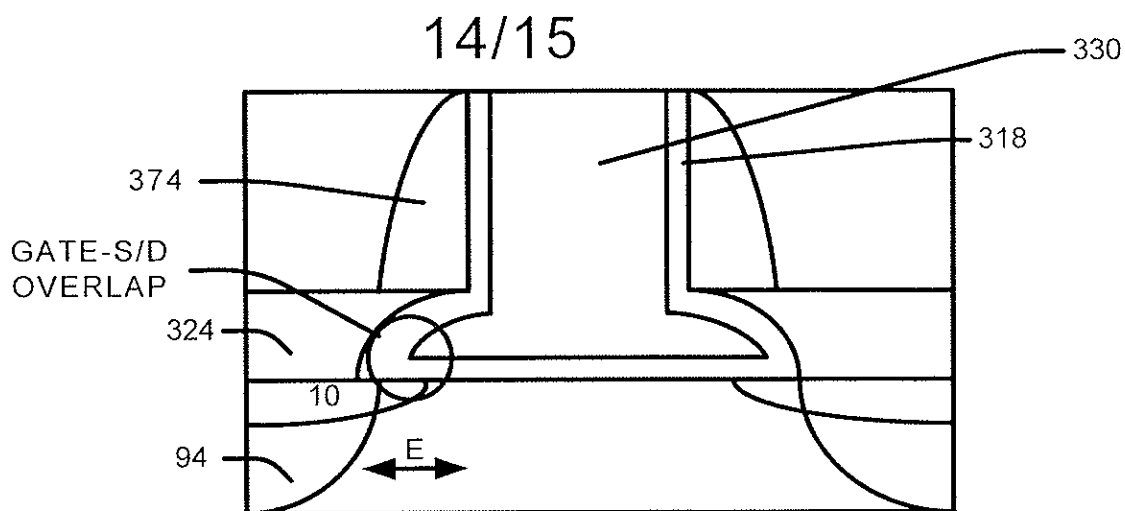


FIGURE 24D

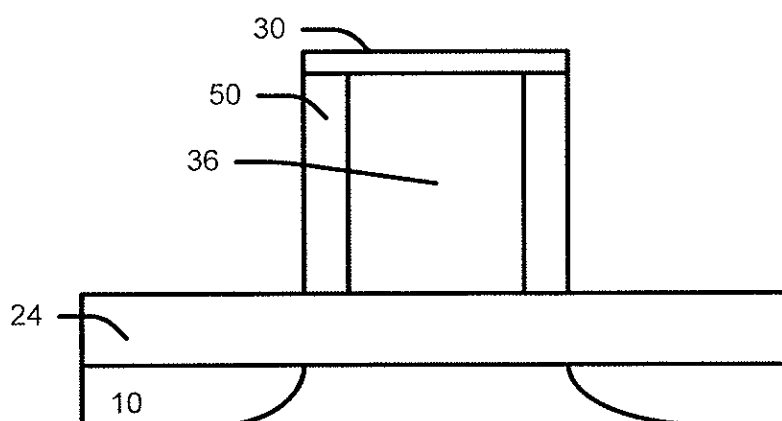


FIGURE 25A-1

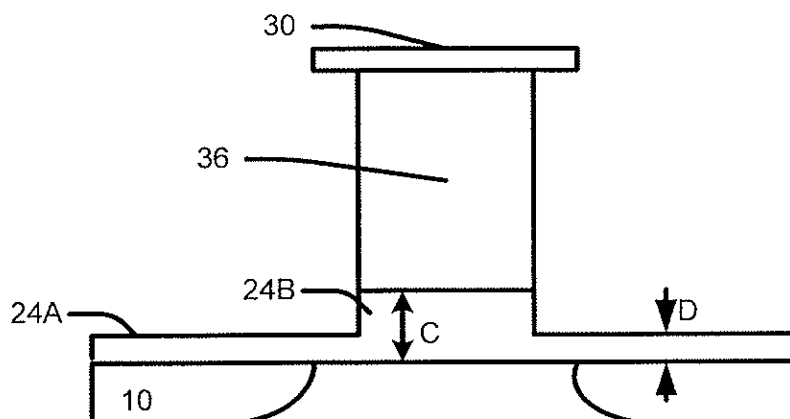


FIGURE 25A-2

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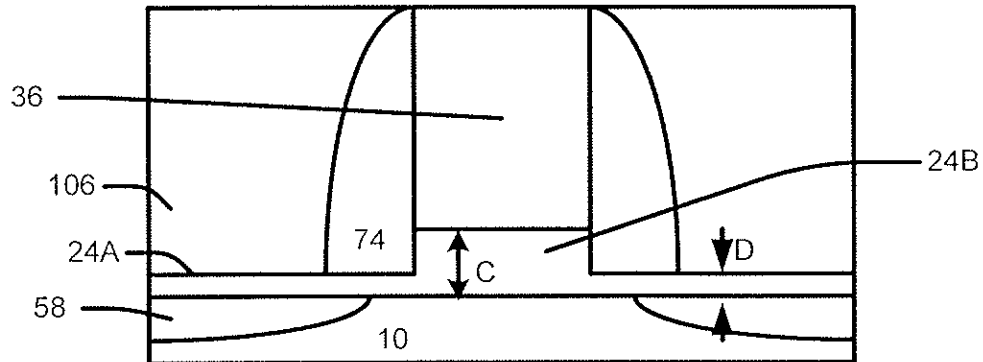


FIGURE 25B

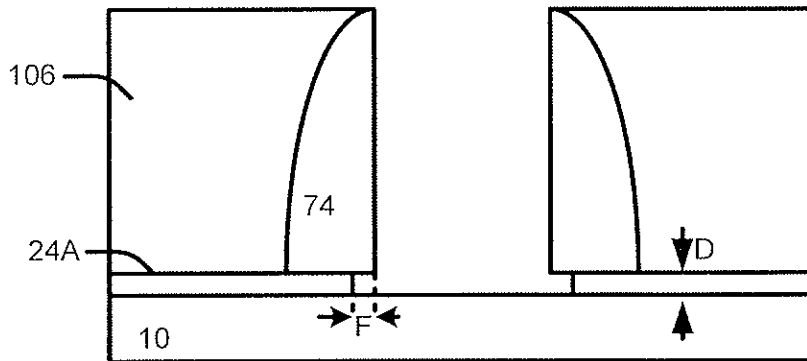


FIGURE 25C

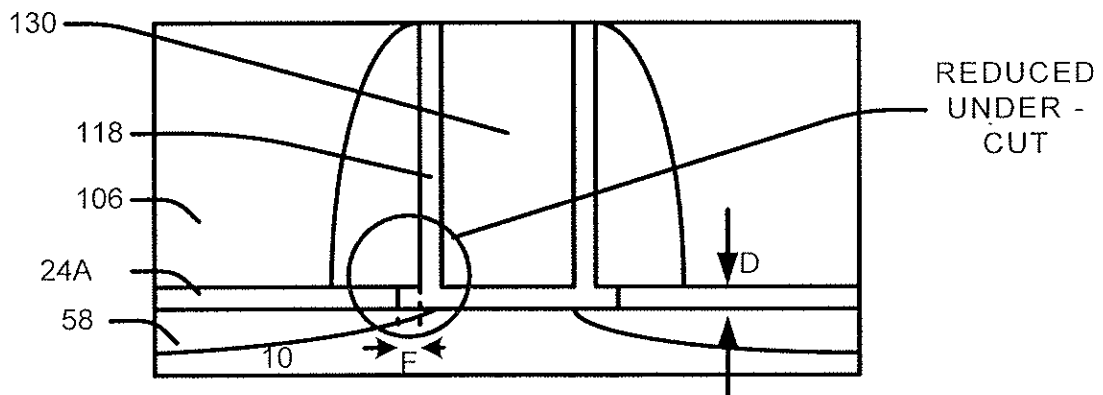


FIGURE 25D