ABSTRACT

METHOD OF FORMING SMALL TRANSISTOR GATES BY USING SELF-ALIGNED REVERSE SPACER AS A HARD MASK

A method of forming narrow gates comprising the following steps. A substrate is provided having an overlying Si_3N_4 or an SiO_2/Si_3N_4 stack gate dielectric layer. A gate material layer is formed over the gate dielectric layer. A hard mask layer is formed over the gate material layer. The hard mask layer and the gate material layer are patterned to form a hard mask/gate material layer stack. A planarized dielectric layer is formed surrounding the hard mask/gate material layer stack. The patterned hard mask layer is removed from over the patterned gate material layer to form a cavity having exposed dielectric layer side walls. Masking spacers are formed on the exposed dielectric layer side walls over a portion of the patterned gate material layer. The patterned gate material layer is etched using the masking spacers as masks to expose a portion of the gate dielectric layer. The planarized dielectric layer is removed. The masking spacers are removed to form narrow gates comprising gate material.

FIGURE 4



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