We claim:

1. A memory device comprising a ecessed access device in a memory array, comprising:

a recess within semiconductive material of a semiconductor substrate, the semiconductive material having an elevationally outermost surface;

a transistor gate dielectric layer lining the recess;

a single conductive metal silicide transistor gate material filling a lower portion of the recess, the metal silicide having an elevationally outermost surface that is elevationally inward of the elevationally outermost surface of the semiconductive material within which the recess is received leaving a remaining volume in an upper portion of the recess, the metal silicide comprising at least two metals; and

an insulative material received within the upper portion of the recess elevationally over and in physical contact with the metal silicide across the elevationally outermost surface of the metal silicide and filling the remaining volume of the recess.

2. The memory device of Claim 1, wherein the at least two metals have opposite diffusivities relative to silicon.

3. The memory device of Claim 1, wherein the metal silicide comprises a first metal selected from the group consisting of nickel, platinum and copper, and a second metal selected from the group consisting of cobalt, titanium and tantalum.

4. The memory device of Claim 1, wherein the recessed access device shares a source with an adjacent recessed access device.

5. The memory device of Claim 1, wherein the recess defines an opening having a width between 25 nm and 75 nm.

6. The memory device of Claim 1, wherein 70-90 at. % of metal in the metal silicide comprises nickel.

7. The memory device of Claim 6, wherein 10-30 at. % of metal in the metal silicide comprises cobalt.

8. A recessed access device, comprising:

a recess within semiconductive material of a semiconductor substrate, the semiconductive material having an elevationally outermost surface;

a transistor gate dielectric layer lining the recess and received against the semiconductive material, the gate dielectric layer being received over and against the semiconductive material laterally outward of the recess;

a single conductive metal silicide transistor gate material having at least two metals, the metal silicide filling a lower portion of the recess, the metal silicide having an elevationally outermost surface that is elevationally inward of the elevationally outermost surface of the semiconductive material within which the recess is received leaving a remaining volume in an upper portion of the recess; and

an insulative material received within the upper portion of the recess and filling the remaining volume of the recess, the insulative material being in physical contact with the gate dielectric layer and in physical contact with the metal silicide across the elevationally outermost surface of the metal silicide, the gate dielectric layer having an elevationally outermost planar surface, the insulative material having an elevationally outermost planar surface which is coplanar with the elevationally outermost planar surface of the gate dielectric layer.

9. The recessed access device of Claim 8, wherein the at least two metals have opposite diffusivities relative to silicon.

10. The recessed access device of Claim 8, wherein the metal silicide comprises a first metal selected from the group consisting of nickel, platinum and copper, and a second metal selected from the group consisting of cobalt, titanium and tantalum.

11. The recessed access device of Claim 8, wherein the recessed access device shares a source with an adjacent recessed access device.

12. The recessed access device of Claim 8, wherein the recess defines an opening having a width between 25 nm and 75 nm.

13. The recessed access device of Claim 8, wherein 70-90 at. % of metal in the metal silicide comprises nickel.

14. The recessed access device of Claim 13, wherein 10-30 at. % of metal in the metal silicide comprises cobalt.

15. The memory device of claim 1 wherein the transistor gate dielectric layer and the insulative material are different in composition.

16. The recessed access device of claim 8 wherein the transistor gate dielectric layer and the insulative material are different in composition.

17. A memory device comprising a recessed access device in a memory array, comprising:

a recess within semiconductive material of a semiconductor substrate, the semiconductive material having an elevationally outermost surface;

a transistor gate dielectric layer lining the recess;

a single conductive metal silicide transistor gate material filling a lower portion of the recess leaving a remaining volume in an upper portion of the recess, the metal silicide having an elevationally outermost surface that is elevationally inward of the elevationally outermost surface of the semiconductive material within which the recess is received, the metal silicide comprising at least two metals; and

an insulative material received within the upper portion of the recess elevationally over and in physical contact with the elevationally outermost surface of the metal silicide and filling the remaining volume of the recess.

18. A memory device comprising a recessed access device in a memory array, comprising:

a recess within semiconductive material of a semiconductor substrate, the semiconductive material having an elevationally outermost surface;

a transistor gate dielectric layer lining the recess;

a single conductive metal silicide transistor gate material filling a lower portion of the recess, the metal silicide having an elevationally outermost surface that is elevationally inward of the elevationally outermost surface of the semiconductive material within which the recess is received leaving a remaining volume in an upper portion of the recess, the metal silicide comprising at least two metals; and

an insulative material received within the upper portion of the recess and filling the remaining volume of the recess, the insulative material being of different composition from that of the transistor gate dielectric, the insulative material being elevationally over and in physical contact with the elevationally outermost surface of the metal silicide, the insulative material being received laterally against the gate dielectric layer.

Claims

1. A method of forming a gate of a recessed access device, comprising:
forming a trench within semiconductive material of a substrate, the trench having a top width that is less than 60 nm;
depositing gate material comprising polysilicon to within the trench;
depositing a metal layer over the semiconductive material, over the polysilicon and within the trench, the metal layer comprising at least two different metals, the two different metals having opposing diffusivities relative to silicon;
subjecting the polysilicon and the metal layer to a silicidation anneal to form metal silicide within the trench; and
forming an insulator over the metal silicide.

2. The method of claim 1 wherein the silicidation anneal transforms all of the polysilicon to metal silicide.

3. The method of claim 1 wherein the silicidation anneal forms the metal silicide at the bottom of the trench.

4. The method of claim 1 wherein the two different metals comprise nickel and cobalt.

5. The method of claim 4 wherein the metal layer has less cobalt than nickel.

6. The method of claim 1 wherein one of the two different metals comprises at least one of Ni, Pt, and Cu, and another of the two different metals comprises at least one of Co, Ti, and Ta.

7. The method of claim 6 wherein the two different metals comprise nickel and titanium.

8. The method of claim 6 wherein the two different metals comprise nickel and tantalum.

9. The method of claim 6 wherein the two different metals comprise platinum and cobalt.

10. The method of claim 6 wherein the two different metals comprise platinum and titanium.

11. The method of claim 6 wherein the two different metals comprise platinum and tantalum.

12. The method of claim 6 wherein the two different metals comprise copper and cobalt.

13. The method of claim 6 wherein the two different metals comprise copper and titanium.

14. The method of claim 6 wherein the two different metals comprise copper and tantalum.

15. The method of claim 1 comprising recessing the metal silicide within the trench.

16. The method of claim 15 comprising after recessing the metal silicide within the trench, forming the insulator within the trench over the metal silicide.