

ABSTRACT

Gate Transition Counter

A gate transition counter. A ring oscillator (10) provides a plurality outputs (103, 105, 107, 109, 111), each delayed from the adjacent output by a gate delay. The outputs (103, 105, 107, 109, 111) of the ring oscillator (10) are captured by an array of latches (20) upon receipt of a halt signal (40). The last latch (140) drives a ripple counter (50). The preferred implementation uses five inverters (102, 104, 106, 108, 110) in the ring oscillator (10) so that each complete cycle of the ring oscillator (10) represents ten gate delays. A ripple counter (10) counts the number of gate delays by ten. The latch outputs R and the ripple counter outputs C can be converted to a binary representation P of the number of gate delays to provide a count in the smallest time increment that can be produced by the circuit.

Figure 1