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(54) SEMICONDUCTOR CHIP FOR HIGH TEMPERATURE PRESSURE CONTACT PACKAGE

(71) We, HEWLETT-PACKARD COMPANY, a corporation organised under the laws of the State of California, United States of America, of 1501 Page Mill Road, Palo Alto, California 94304, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a semiconductor chip. The invention may be embodied as a Schottky barrier diode chip which is capable of withstanding temperatures of the order of 700°C and pressures commonly developed in a DO-35 semiconductor package when such chips are sealed therein. In the chips described herein, the pressure applied to the chip by the package is diverted from the active region whilst reliable electrical contact is assured without damage to the chip or degradation of its electrical characteristics.

The electrical characteristics of certain semiconductor devices such as Schottky barrier diodes are significantly degraded as a function of pressure applied to the junction area. Such devices therefore require extensive multi-piece packaging schemes to avoid damage to the chip or degradation of the electrical characteristics thereof. Such a packaging method is shown, for example, in U.S. Patent 3,178,796.

The DO-35 package is a reliable, hermetic, glass-to-metal seal, semiconductor package consisting of two identical stud-leads 10 (hereinafter referred to as studs and typically of Dumet or other suitable lead material) and a glass sleeve 12 as shown in Figure 1. While its assembly is simple, fast and efficient, the package does rely on pressure contact of the studs directly to the semiconductor chip for electrical connection of, for example, the anode and cathode of a diode to the package leads. After assembly, the entire assembled unit including chip 11 is heated to a temperature of approximately 700°C to obtain the hermetic glass-to-metal seal. As the package cools, additional pressure is applied to the chip as a result of the contraction of the glass as it cools to room temperature. Schottky barrier diodes of conventional design (contact button on top of the junction area) show degraded characteristics after this sealing process.

The effects of high temperature on the metallization and chemical integrity of the diode chip must also be considered. For a Schottky barrier diode, the metallization must achieve the desired barrier height and exhibit good adhesion to Si, SiO_2 and Si_3N_4. In addition, undesirable chemical reactions between package impurities and the diode chip during the sealing process must be prevented.

The present invention provides a semiconductor chip having at least one active region for use in a sealed high-temperature, pressure-contact lead package, said semiconductor chip comprising; a layer of a first material covering a surface of the semiconductor chip, except for at least a portion of the active region which is bounded by said surface, said layer being provided for chemically insulating said surface of the semiconductor chip; a layer of a second material covering the first layer of the first material for chemically insulating the semiconductor chip so as to prevent reaction with package impurities; a layer of the first material covering the layer of the second material for enhancing adhesion thereof with subsequent layers; a layer of a third material covering the last-mentioned layer of the first material for providing insulation; and a layer of electrically conducting material covering the entire exposed portion of the active region of the semiconductor chip and covering a portion of the layer of third material for physically and electrically contacting a lead, said layer of electrically conducting material including extensions each connected to respective contact pads disposed so as to contact said lead at a relatively substantial distance from the active region thereby to transmit pressure of the contacting leads away from

the active region, said contact pads having greater thickness than the other portions of said layer of electrically conducting material.

According to one embodiment of the invention, a relatively thick glass layer covers the surface of a diode chip except for the active region bounded by said surface. The chip is contained in an elongated glass sleeve having electrically conductive studs at each end, the studs making respective electrical contact with an anode and a cathode of the chip. The glass sleeve is heated to a temperature required for hermetically sealing the sleeve to the studs. Additional pressure developed by the glass sleeve, as it contracts during cooling from the sealing temperature, is transferred via the studs and the glass layer to the contact pads remote from the active region.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which:—

Figure 1 is a simplified cross-sectional view of an assembled DO-35 semiconductor package.

Figure 2 is a cross-sectional view of a Schottky barrier diode chip used in several embodiments of the present invention.

Figure 3 is a cross-sectional view of a Schottky barrier diode chip constructed according to one embodiment of the present invention.

Figure 4a is a cross-sectional view of a Schottky barrier diode chip constructed according to another embodiment of the present invention.

Figure 4b is a top view of the embodiment of Figure 4a.

Figure 5 is a cross-sectional view of a Schottky barrier diode chip constructed according to another embodiment of the present invention.

Referring to Figure 2 a Schottky barrier diode chip is first formed of an n^+ substrate 20 on which contiguous regions 22, 23, 24 and 25 are deposited. A P-type guard ring 26 is formed in N-type epitaxial layer 22. A buffer layer 27 of silicon dioxide (SiO_2) is provided over P-type guard ring 26 and region 25. Regions 23 and 25 also comprise SiO_2. Region 24 is formed of silicon nitride (Si_3N_4) and will be discussed later in this specification. This configuration of the active semiconductor region 37 (Figure 3) of the diode chip is unaffected by the packaging configurations of the present invention.

After the diode chip is formed as shown in Figure 2, it is ready for modification in accordance with the present invention. As shown in Figure 3, one embodiment includes a layer of glass 30 deposited over the entire surface of chip 11 except in the immediate area of the active Schottky barrier region 37. The thickness of the glass layer 30 reduces semiconductor chip capacitance. A substantially uniform layer of metallization 31 for electrical contact to the anode of the diode is then applied over the entire active barrier region 37, continuing over the top of the glass layer where it forms contact pads remote from the region 37. The contact pads are thicker than the other portions of the layer 31, as shown by the prominent regions at each side of the active region 37, and are connected by extensions to the metallization over region 37.

Metallization 31 is a deposition of tungsten (W) followed by a deposition of silver (Ag). Ag is used for reliable electrical contact with a stud 10. Tungsten is used to control the Schottky barrier height and protect against metallurgical reaction of Ag with the semiconductor chip at the package sealing temperature. In the packaged configuration of the present invention, one surface 33 of modified chip 35 is placed on one stud, now referred to as the cathode stud. After glass sleeve 12 is in place around the cathode stud, the anode stud is inserted to make contact with metallization 31. Thus, modified diode chip 35 is sandwiched between two studs 10 as shown in Figure 1, the physical contact of studs 10 being effective for making electrical contact with the anode and cathode of diode chip 35. The entire assembly is then heated to the required temperature to hermetically seal glass sleeve 12 to studs 10. As sleeve 12 cools it contracts, hence increasing the pressure which studs 10 apply to the contact pads of chip 35. However that increased pressure is transmitted via glass layer 30 to the chip a substantial distance away from active barrier region 37, yet electrical contact with the anode portion of diode chip 35 is maintained via metallization 31.

Of course other combinations of metallization material can be used so long as the objectives of controlling barrier height, contacting the studs and withstanding high temperature sealing of the package are achieved. For example, instead of a W-Ag metallization, the metallization could comprise W-Ti-Ag, W-Cr-Au or W-Cr-Ag.

Referring now to Figures 4a and 4b, another embodiment of diode chip 46 constructed according to the present invention is shown. Construction of the diode is similar to that shown in and described in Figure 1 but without glass layer 30. Prior to metallization a relatively thick layer 42 of SiO_2 is deposited over the entire surface of chip 11 with the exception of barrier region 37. The commercially available "ROTOX" process is used for the deposition. Thereafter, metallization 16, which includes a layer of W, is deposited, substantially covering the barrier region but having fingers 43 leading to coplanar electrical contact pads 45 remotely disposed at a relatively substantial

distance from barrier region 37. The contact pads 45 comprise a deposition of titanium (Ti) followed by a layer of Ag and are built up by electroplating additional Ag to a thickness significantly greater than metal fingers 43. For assembly, as with the configuration of Figure 3, surface 44 of modified chip 46 is placed on one stud and, after the glass sleeve 12 is in place, the second stud is inserted to make electrical contact with one or more of the four electrical contact pads 45. This chip configuration requires fewer process steps to build than the configuration of Figure 1.

Referring to Figure 5, a layer 57 of Si_3N_4 is added to a chip similar to the chip shown in Figures 4a and 4b prior to applying metallization 16 to form another configuration of the present invention. The thickness of layer 57 reduces semiconductor chip capacitance. The chip comprises a substrate 50 on which a contiguous N-type expitaxial layer 52 is grown and in which a P-type guard ring 51 is formed. Layers 54 and 56 are SiO_2 and layers 55 and 57 are Si_3N_4. Metallization 16 leading to contact pads is then applied over the active region (analogous to active region 37 shown in Figure 3). and layer 57. Alternatively, layer 57 may be formed of SiO_2 highly doped with either phosphorous or boron, or of any other dielectric material which provides an ionic barrier against impurities formed during high temperature sealing of the package.

One source of chemical impurities during the high temperature sealing process is sodium tetraborate which is used as a flux. The passivation of Si_3N_4 over the entire surface of chip 11 acts as a barrier to such impurities which would otherwise cause degradation of performance of the devices with time. This passivation layer is represented as region 24 in Figure 2 and regions 55 and 57 in Figure 5.

While described for use with the Schottky barrier diode chip, the configuration of the present invention is useful with any semiconductor chip, particularly those which are sensitive to temperatures and pressures developed while being enclosed and sealed in the DO-35 package.

WHAT WE CLAIM IS:—

1. A semiconductor chip having at least one active region for use in a sealed high temperature, pressure contact lead package, said semiconductor chip comprising a layer of first material, covering a surface of the semiconductor chip, except for at least a portion of the active region which is bounded by said surface, said layer being provided for chemically insulating said surface of the semiconductor chip; a layer of a second material covering the first layer of the first material for chemically insulating the semiconductor chip so as to prevent reaction with package impurities; a layer of the first material covering the layer of the second material for enhancing adhesion thereof with subsequent layers; a layer of a third material covering the last mentioned layer of the first material for providing insulation; and a layer of electrically conducting material covering the entire exposed portion of the active region of the semiconductor chip and covering a portion of the layer of third material for physically and electrically contacting a lead, said layer of electrically conducting material including extensions each connected to respective contact pads disposed so as to contact said lead at a relatively substantial distance from the active region thereby to transmit pressure of the contacting leads away from the active region, said contact pads having greater thickness than the other portions of said layer of electrically conducting material.

2. A semiconductor chip as claimed in claim 1 wherein the first material is silicon dioxide; the second material is silicon nitride; the third material is glass; and the layer of conducting material includes a first layer of tungsten and a second layer of silver.

3. A semiconductor chip as in claim 1 wherein the thickness of the layer of conducting material is substantially uniform over its entire area.

4. A semiconductor chip as in claim 1 wherein the layer of conducting material includes four narrow extensions connected to respective contact pads.

5. A semiconductor chip as in claim 4 wherein the layer of conducting material includes four narrow extensions thereof each connecting to one contact pad.

6. A semiconductor chip as in claim 4 wherein the first and third material is silicon dioxide; the second material is silicon nitride; and the layer of conducting material includes a first layer of tungsten, a second layer of titanium and a third layer of silver.

7. A semiconductor chip as in claim 4 wherein the third material is the same as the second material.

8. A Schottky barrier diode chip substantially as herein described with reference to Fig. 3 of the accompanying drawings.

9. A Schottky barrier diode chip substantially as herein described with reference to Figs. 4a and 4b of the accompanying drawings.

10. A Schottky barrier diode chip substantially as herein described with reference to Fig. 5 of the accompanying drawings.

11. A semiconductor package comprising an elongated glass sleeve having an electrically conductive stud at each end, said sleeve containing the chip according to any one of

distance from barrier region 37. The contact pads 45 comprise a deposition of titanium (Ti) followed by a layer of Ag and are built up by electroplating additional Ag to a thickness significantly greater than metal fingers 43. For assembly, as with the configuration of Figure 3, surface 44 of modified chip 46 is placed on one stud and, after the glass sleeve 12 is in place, the second stud is inserted to make electrical contact with one or more of the four electrical contact pads 45. This chip configuration requires fewer process steps to build than the configuration of Figure 1.

Referring to Figure 5, a layer 57 of Si_3N_4 is added to a chip similar to the chip shown in Figures 4a and 4b prior to applying metallization 16 to form another configuration of the present invention. The thickness of layer 57 reduces semiconductor chip capacitance. The chip comprises a substrate 50 on which a contiguous N-type expitaxial layer 52 is grown and in which a P-type guard ring 51 is formed. Layers 54 and 56 are SiO_2 and layers 55 and 57 are Si_3N_4. Metallization 16 leading to contact pads is then applied over the active region (analogous to active region 37 shown in Figure 3). and layer 57. Alternatively, layer 57 may be formed of SiO_2 highly doped with either phosphorous or boron, or of any other dielectric material which provides an ionic barrier against impurities formed during high temperature sealing of the package.

One source of chemical impurities during the high temperature sealing process is sodium tetraborate which is used as a flux. The passivation of Si_3N_4 over the entire surface of chip 11 acts as a barrier to such impurities which would otherwise cause degradation of performance of the devices with time. This passivation layer is represented as region 24 in Figure 2 and regions 55 and 57 in Figure 5.

While described for use with the Schottky barrier diode chip, the configuration of the present invention is useful with any semiconductor chip, particularly those which are sensitive to temperatures and pressures developed while being enclosed and sealed in the DO-35 package.

WHAT WE CLAIM IS:—

1. A semiconductor chip having at least one active region for use in a sealed high temperature, pressure contact lead package, said semiconductor chip comprising a layer of first material, covering a surface of the semiconductor chip, except for at least a portion of the active region which is bounded by said surface, said layer being provided for chemically insulating said surface of the semiconductor chip; a layer of a second material covering the first layer of the first material for chemically insulating the semiconductor chip so as to prevent reaction with package impurities; a layer of the first material covering the layer of the second material for enhancing adhesion thereof with subsequent layers; a layer of a third material covering the last mentioned layer of the first material for providing insulation; and a layer of electrically conducting material covering the entire exposed portion of the active region of the semiconductor chip and covering a portion of the layer of third material for physically and electrically contacting a lead, said layer of electrically conducting material including extensions each connected to respective contact pads disposed so as to contact said lead at a relatively substantial distance from the active region thereby to transmit pressure of the contacting leads away from the active region, said contact pads having greater thickness than the other portions of said layer of electrically conducting material.

2. A semiconductor chip as claimed in claim 1 wherein the first material is silicon dioxide; the second material is silicon nitride; the third material is glass; and the layer of conducting material includes a first layer of tungsten and a second layer of silver.

3. A semiconductor chip as in claim 1 wherein the thickness of the layer of conducting material is substantially uniform over its entire area.

4. A semiconductor chip as in claim 1 wherein the layer of conducting material includes four narrow extensions connected to respective contact pads.

5. A semiconductor chip as in claim 4 wherein the layer of conducting material includes four narrow extensions thereof each connecting to one contact pad.

6. A semiconductor chip as in claim 4 wherein the first and third material is silicon dioxide; the second material is silicon nitride; and the layer of conducting material includes a first layer of tungsten, a second layer of titanium and a third layer of silver.

7. A semiconductor chip as in claim 4 wherein the third material is the same as the second material.

8. A Schottky barrier diode chip substantially as herein described with reference to Fig. 3 of the accompanying drawings.

9. A Schottky barrier diode chip substantially as herein described with reference to Figs. 4a and 4b of the accompanying drawings.

10. A Schottky barrier diode chip substantially as herein described with reference to Fig. 5 of the accompanying drawings.

11. A semiconductor package comprising an elongated glass sleeve having an electrically conductive stud at each end, said sleeve containing the chip according to any one of

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the preceding claims wherein said studs make respective electrical contact with an anode and a cathode of said chip, the package being produced by heating said sleeve to a temperature required for hermetically sealing said sleeve to said studs whereby, as the sleeve cools, it contracts to increase the pressure which said studs apply to said chip.

12. A semiconductor package according to claim 11 wherein said sleeve and said studs form a DO-35 package.

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