(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 July 2004 (29.07.2004)

PCT

(10) International Publication Number
WO 2004/064148 A1

(51) International Patent Classification[7]: H01L 21/8242

(21) International Application Number:
PCT/US2003/000562

(22) International Filing Date: 8 January 2003 (08.01.2003)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MANDELMAN, Jack, A.** [US/US]; 11 Claremont Drive, Flat Rock, NC 28731 (US). **GAMBINO, Jeffrey, P.** [US/US]; 98 Huntley Road, Westford, VT 05494 (US). **WANG, Geng** [US/US]; 15 Whitegate Drive, Apt. D, Wappingers Falls, NY 12590 (US).

(74) Agent: **BLECKER, Ira, D.**; International Business Machines Corporation, Dept. 18G, Bldg. 300/482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

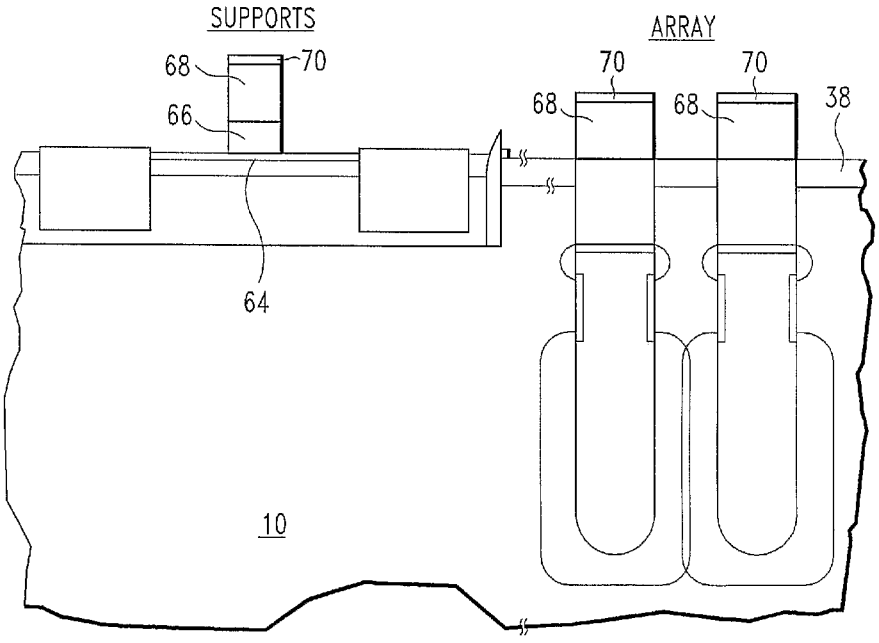
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declaration under Rule 4.17:**
— *of inventorship (Rule 4.17(iv)) for US only*

**Published:**
— *with international search report*

*[Continued on next page]*

(54) Title: HIGH PERFORMANCE EMBEDDED DRAM TECHNOLOGY WITH STRAINED SILICON




(57) Abstract: Semiconductor devices are fabricated in a strained layer region and strained layer-free region of the same substrate. A first semiconductor device, such as a memory cell, e.g. a deep trench storage cell, is formed in a strained layer-free region of the substrate. A strained layer region is selectively formed in the same substrate. A second semiconductor device (66, 68, 70), such as an FET, e.g. an MOSFET logic device, is formed in the strained layer region.

WO 2004/064148 A1

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*