What is claimed is:

1. A search circuit comprising:

a content-addressable memory (CAM) comprising a plurality of CAM cells configured to store a plurality of entry data, each entry data comprising a first bit corresponding to a least significant bit through a K-th bit corresponding to a most significant bit, the CAM configured to provide a plurality of matching signals indicating whether each of the plurality of entry data matches searching data; and

a CAM controller configured to perform a partial searching operation such that the CAM controller applies comparison bits corresponding to a portion of the first through K-th bits that is less than all of the first through K-th bits as the searching data to the CAM and searches for target entry data among the plurality of entry data based on the plurality of matching signals indicating that the corresponding bits of the target entry data match the comparison bits.

2. The search circuit of claim 1, wherein the CAM controller is further configured to repeat the partial searching operation by changing the comparison bits until the target entry data are determined.

3. The search circuit of claim 1, wherein the CAM controller is further configured to repeat the partial searching operation by increasing a number of the comparison bits one by one in a direction from the K-th bit to the first bit to determine maximum entry data having a maximum value among the entry data or to determine minimum entry data having a minimum value among the entry data as the target entry data.

4. The search circuit of claim 3, wherein the CAM controller is further configured to determine values of (i+1) comparison bits of an (i+1)-th partial searching operation based on the plurality of matching signals of an i-th partial searching operation having i comparison bits, where i is a natural number.

5. The search circuit of claim 4, wherein the CAM controller is further configured to not perform the (i+1)-th partial searching operation responsive to only one of the plurality of matching signals being activated by the i-th partial searching operation.

6. The search circuit of any one of claims 3 to 5, wherein, responsive to the target entry data being the maximum entry data, the CAM controller is further configured to perform a first partial searching operation by applying the K-th comparison bit having a value of 1 to the CAM.

7. The search circuit of claim 6, wherein, responsive to the target entry data being the maximum entry data having the maximum value among the entry data, the CAM controller is further configured to perform the (i+1)-th partial searching operation by applying the K-th through (K-i+1)-th comparison bits to the CAM such that the CAM controller is further configured to set the value of the (K-i+1)-th comparison bit to 1 responsive to at least one of the plurality of matching signals being activated by the i-th partial searching operation, and is further configured to set the value of the (K-i+1)-th comparison bit to 0 and the value of the (K-i)-th comparison bit to 1 responsive to all of the plurality of matching signals being deactivated by the i-th partial searching operation.

8. The search circuit of claim 7, wherein, responsive to only one of the plurality of matching signals being activated, the CAM controller is further configured to determine the entry data corresponding to the only one activated matching signal as the maximum entry data having the maximum value among the entry data.

9. The search circuit of any one of claims 3 to 8, wherein, responsive to the target entry data being the minimum entry data having the minimum value among the entry data, the CAM controller is further configured to perform a first partial searching operation by applying the K-th comparison bit having a value of 0 to the CAM.

10. The search circuit of claim 9, wherein, responsive to the target entry data being the minimum entry data having the minimum value among the entry data, the CAM controller is further configured to perform the (i+1)-th partial searching operation by applying the K-th through (K-i+1)-th comparison bits to the CAM such that the CAM controller is further configured to set the value of the (K-i+1)-th comparison bit to 0 when at least one of the plurality of matching signals is activated by the i-th partial searching operation, and is further configured to set the value of the (K-i+1)-th comparison bit to 1 and the value of the

(K-i)-th comparison bit to 0 when all of the plurality of matching signals are deactivated by the i-th partial searching operation.

11. The search circuit of claim 10, wherein, responsive to only one of the plurality of matching signals being activated, the CAM controller is further configured to determine the entry data corresponding to the only one activated matching signal as the minimum entry data having the minimum value among the entry data.

12. The search circuit of any one of claims 1 to 11, wherein the CAM comprises a binary CAM (BCAM) that stores a value of 0 or a value of 1 to each bit of the first through K-th bits of the plurality of entry data.

13. The search circuit of claim 12, wherein the CAM cells corresponding to each of the first through K-th bits of the plurality of entry data are configured to receive each bit of the searching data through a normal searching line and a complementary searching line.

14. The search circuit of claim 13, wherein the CAM controller is further configured to apply a value of 1 to one of the normal searching line and the complementary searching line and to apply a value of 0 to the other of the normal searching line and the complementary searching line, with respect to each of the comparison bits among bits of the searching data, and

wherein the CAM controller is further configured to apply the value of 1 or the value of 0 to both of the normal searching line and the complementary searching line, respectively, with respect to each of non-comparison bits among the bits of the searching data.

15. A memory system comprising:

a memory cell array comprising a plurality of memory cells;

a hammer address management circuit configured to determine a hammer address of the memory cell array that is accessed intensively; and

a refresh controller configured to perform a hammer refresh operation to refresh a first row of the memory cell array that is physically adjacent to a second row of the memory cell array corresponding to the hammer address, wherein the hammer address management circuit comprises:

an address storage configured to store a plurality of row addresses based on an access address signal;

a content-addressable memory (CAM) comprising a plurality of CAM cells configured to store a plurality of access count data indicating a plurality of access counts of the plurality of row addresses, each access count data comprising a first bit corresponding to a least significant bit through a K-th bit corresponding to a most significant bit, the CAM configured to provide a plurality of matching signals indicating whether each of the plurality of access count data matches searching data;

a CAM controller configured to perform a partial searching operation such that the CAM controller applies comparison bits corresponding to a portion of the first through K-th bits that is less than all of the first through K-th bits as the searching data to the CAM and searches for target count data among the plurality of access count data based on the plurality of matching signals indicating that the corresponding bits of the target count data match the comparison bits; and

an address controller configured to provide the hammer address among the plurality of row addresses stored in the address storage, based on a result of searching for the target count data.

16. The memory system of claim 15, wherein the CAM controller is further configured to repeat the partial searching operation by increasing a number of the comparison bits one by one in a direction from the K-th bit to the first bit to determine maximum count data having a maximum value among the access count data or minimum count data having a minimum value among the access count data as the target count data.

17. The memory system of claim 15, wherein the CAM controller is further configured to repeat the partial searching operation to determine maximum count data having a maximum value among the plurality of access count data as the target count data, and

wherein the address controller is further configured to provide the row address corresponding the maximum count data as the hammer address.

18. The memory system of claim 15, wherein the CAM controller is further configured to repeat the partial searching operation to determine maximum count data having a maximum value among the plurality of access count data as the target count data, and

wherein the address controller is further configured to store a new row address in the address storage to replace the row address corresponding to the minimum count data with the new row address.

19. The memory system of any one of claims 15 to 18, wherein the CAM comprises a binary CAM (BCAM) that stores a value of 0 or a value of 1 to each bit of the first through K-th bits of the plurality of access count data.

20. A hammer address management circuit of a memory system, comprising:

an address storage configured to store a plurality of row addresses based on an access address signal provided to a memory device;

a content-addressable memory (CAM) comprising a plurality of CAM cells configured to store a plurality of access count data indicating a plurality of access counts of the plurality of row addresses, each access count data including a first bit corresponding to a least significant bit through a K-th bit corresponding to a most significant bit, the CAM configured to provide a plurality of matching signals indicating whether each of the plurality of access count data matches searching data;

a CAM controller configured to perform a partial searching operation such that the CAM controller applies comparison bits corresponding to a portion of the first through K-th bits that is less than all of the first through K-th bits as the searching data to the CAM and search for target count data among the plurality of access count data based on the plurality of matching signals indicating that the corresponding bits of the target count data match the comparison bits; and

an address controller configured to provide a hammer address of the memory device that is accessed intensively, based on a result of searching for the target count data.