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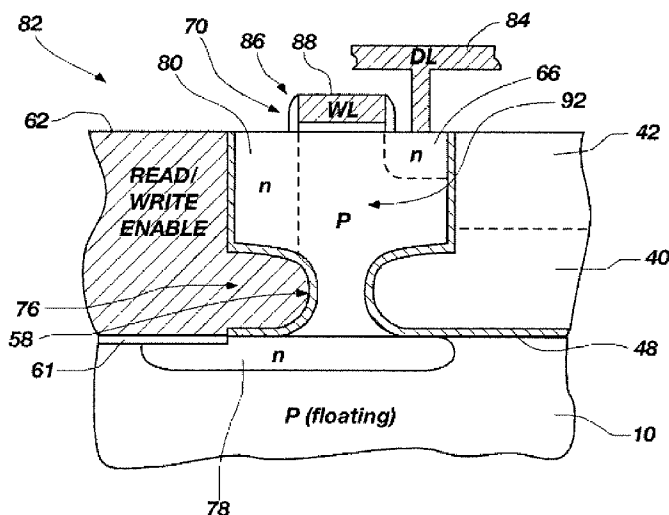


FIG. 11

(57) Abstract: A capacitor-less floating-body memory cell, memory device, system and process of forming the capacitor-less memory cell includes forming the memory cell (82) in a active area of a substantially physically isolated portion of the bulk semiconductor substrate (10). A pass transistor (70) is formed on the active area for coupling with a word line (88). The capacitor-less memory cell further includes a read/write enable transistor (76) vertically configured along at least one vertical side of the active area, sharing a floating source/drain region (80) with the pass transistor, and operable during a reading of a logic state with the logic state being stored as charge in a floating body area of the active area, causing different determinable threshold voltages for the pass transistor.

INTERNATIONAL SEARCH REPORT

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Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

A capacitor-less floating-body memory cell, memory device, system and process of forming the capacitor-less memory cell includes forming the memory cell (82) in a active area of a substantially physically isolated portion of the bulk semiconductor substrate (10). A pass transistor (70) is formed on the active area for coupling with a word line (88). The capacitor-less memory cell further includes a read/write enable transistor (76) vertically configured along at least one vertical side of the active area, sharing a floating source/drain region (80) with the pass transistor, and operable during a reading of a logic state with the logic state being stored as charge in a floating body area of the active area, causing different determinable threshold voltages for the pass transistor.