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COMPLETE SPECIFICATION

Field-effect Devices and Methods of Fabrication thereof

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to field-effect transistors and a methods of fabricating them.

According to the present invention there is provided a field-effect transistor comprising a substrate of semiconductor material of one conductivity type, a low resistivity channel of semiconductor material of the opposite conductivity type, in said substrate, said channel being substantially free of dopants of said opposite conductivity type, a source of semiconductor material of said opposite conductivity type in said substrate contacting said channel, a drain of semiconductor material of said opposite conductivity type in said substrate contacting said channel, and a gate electrode opposite to and spaced from said channel by an insulating layer of high resistivity material.

In an electrical circuit comprising a plurality of field-effect transistors, according to the invention, the substrate of semiconductor material includes a plurality of layers of converted substrate material such as oxides of said substrate material, each layer being respectively separated from the bulk of said substrate by a different low resistivity channel, a plurality of sources and drains, each of said sources and drains except for the end ones being respectively connected to two different channels and acting as a source for one channel and a drain for the other of said two different channels, and a plurality of gate electrodes, each of said gate electrodes being arranged upon a respectively different one of

said plurality of layers and being spaced from said one layer's respective low resistivity channel.

The present invention also provides a method of fabricating a field-effect transistor comprising the steps of: producing at least two spaced insulating layers portions on a surface of a semiconductor substrate of high resistivity material and having one conductivity type, said layer portions containing impurities of opposite conductivity type to said substrate, producing a reacted region in said substrate between said insulating layer portions, said reacted region including a converted layer of the substrate material, such as an oxide of said substrate, and a low resistivity channel between the bulk of said body and said converted layer of substrate material, causing said impurities to diffuse from said layer portions into said substrate to form low resistivity diffused regions contiguous with and defining the ends of said channel, and then producing an electrode on said converted layer of substrate material opposite to and spaced from said channel.

A transistor fabricated in accordance with the present invention is capable of operation in either or both the depletion and enhancement modes of operation. The transfer characteristics of the transistor is continuous over a relatively large range of gate voltages, and the drain current for zero gate voltage can be selected throughout a substantial current range by relatively simple changes in the method of fabrication.

By the method of the invention, the channel, the layer of converted body material, the source, and the drain may all be produced during the same step, following only a single masking of the semiconductor body. The characteristics of the transistor may be modified by a suitable choice of the semiconductor material, its resistivity and its conductivity type; by the selection of the im-

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purity in the deposited layer portions and its concentration; and by the choice of time, temperature, and atmosphere used during the step of producing the reacted region.

5 In the accompanying drawings:

FIGURE 1 is a diagrammatic view, partially in section, of a first embodiment of a field-effect transistor according to the invention having a circular or ring geometry and a typical biasing arrangement for operating the transistor,

FIGURE 2 is a family of curves illustrating the drain characteristics of the embodiment of FIGURE 1,

FIGURE 3 is a diagrammatic view, partially in section, of a second embodiment of the invention showing several field-effect transistors in series, each having a ladder geometry and a biasing arrangement for operating one of the transistors,

FIGURES 4A, 4B and 4C are partial sectional views of structures illustrating a method for fabricating a third embodiment of field-effect transistors according to the invention, having a ladder geometry similar to the embodiment of FIGURE 3, but having a different gate electrode design,

FIGURE 5 is a family of curves illustrating the drain characteristics of the embodiment of FIGURE 4C.

FIGURE 6 is a family of curves illustrating the drain characteristics of a fourth embodiment of field-effect transistors according to the invention, having a geometry similar to the embodiment of FIGURE 4C, except that the drain characteristics have been modified by a longer heating in dry oxygen,

FIGURE 7 is a family of curves illustrating the drain characteristics of a fifth embodiment of a field-effect transistor according to the invention, having a geometry similar to the embodiment of FIGURE 4C except that the drain characteristics have been modified by a subsequent annealing in dry nitrogen,

FIGURE 8 is a plan of a sixth embodiment of the invention, showing several field-effect transistors having a modified gate geometry, and

FIGURE 9 is a family of curves illustrating the drain characteristics of the embodiment of FIGURE 8.

Similar reference numerals are used for similar elements throughout the several FIGURES.

The first embodiment of a unipolar field-effect transistor 21 shown in FIGURE 1 has a circular or ring geometry. The transistor 21 includes a base 23 of semiconductor material preferably of high resistivity material which may be single crystal or polycrystalline. The material may be any one of the semiconductor materials used to prepare transistors in the semiconductor art.

The base 23 includes a reacted region 65 having a layer 25 of converted body material

and a low resistivity channel 27 between the bulk of the base 23 and an insulating layer 25. The layer 25 is of high resistivity material. For purposes of illustration, the base 23 in FIGURE 1 is a single crystal body of P-type silicon having a resistivity of approximately 200 ohm-cm. The layer 25 in this embodiment has generally a ring shape and is produced by oxidizing a portion of the surface of the body 23. The layer 25 is approximately 2000 Å thick and consists essentially of pure silicon oxide produced by completely oxidizing silicon of the body 23.

The low resistivity channel 27 is produced at the same time as the layer 25 and is sometimes referred to as an inversion layer. The channel 27 is believed to have a low resistivity by virtue of attracting free charge carriers thereto, which compensate for unbalanced electronic charges in the partially converted semiconducting material of the channel. A gate electrode 29, preferably of a metal such as aluminium, rests on the layer 25 opposite to and spaced from the channel 27.

A source 31 contacts the outer periphery of the channel 27. A drain 33 contacts the inner periphery of the channel 27. The length of the channel 27, which is the distance between the outer and inner peripheries of the channel 27, is approximately 0.0005 inch. As illustrated, the source 31 and the drain 33 are regions of the body 23 into which N-type impurities have been diffused to render them conducting.

A source electrode 35, of a generally ring shape, and defined by adjacent deposited insulating portions 39 and 41, overlies and contacts a part of the source 31. A generally disc shaped drain electrode 37, defined by adjacent deposited insulating portion 43, overlies and contacts a part of the drain connection 33. The source and drain electrodes 35 and 37 are preferably of a metal, such as aluminium, and may be produced in the same step and of the same material as the gate electrode 29. The deposited insulating portions 39, 41 and 43 are of deposited silicon dioxide approximately 0.1 to 10 microns thick, and preferably one micron thick.

FIGURE 1 also illustrates a biasing arrangement for operating the transistor 21. The source electrode 35 is connected to ground potential 51 by a source conductor 53. The gate electrode 29 is connected to a terminal of a variable supply 55 of gate voltage, V_g , by a gate conductor 57, the other terminal of the supply 55 of gate voltage being grounded. The drain electrode 37 is connected to a terminal of an adjustable supply 59 of drain voltage, V_d , by a drain conductor 61 through a load 63, the other terminal of the supply 59 of drain voltage being grounded. Output terminals 65 are connected to the ends of the load 63. It should be noted that the adjustable supplies 55 and 59

may be reduced to zero output or have their polarities reversed, if desired.

In one mode of operation, the drain voltage, V_d , is adjusted to a desired value by varying the supply 59. The gate voltage, V_g , which is the input or signal to the transistor, and which may be Direct Current, (DC) Alternating Current, (AC) in frequencies up to 100 mc, or pulses, is provided from the gate voltage supply 55, or may be impressed in addition to a fixed bias value. Although not illustrated, a small oscillator or input signal terminals may be arranged in series with adjustable supply 55, if desired, for this purpose. Drain current, I_d , which is the output current of the transistor, flows from supply 59 through the drain conductor 61 to the drain electrode 37, then from the drain electrode 37 through the drain 33, the channel 27, the source 31 and the source electrode 35, and then from the source electrode 35 through the source conductor 53 to the ground 51 which is connected to the other terminal of supply 59. The drain current, I_d , is a replica of the gate voltage, V_g . The output power may be many times the input power and the input impedance may be many times the output impedance. Thus, the transistor may be used to translate from a higher impedance input to a lower impedance output, to amplify the input power, or both to translate and to amplify.

FIGURE 2 is a family of curves illustrating the drain characteristics (drain current I_d plotted against drain voltage, V_d) of the unit of transistor and biasing arrangement of FIGURE 1. Each curve was made with the gate voltage, V_g , held constant at the indicated value in volts and the source electrode 35 connected to ground. Increasing values of drain voltage, V_d , (in volts) were applied to the drain and the corresponding drain currents, I_d , (in milliamperes) were measured. The gate input impedance is capacitive at low frequencies. Time constant measurements indicate a leakage resistance in the range of 10^{14} to 10^{16} ohms. FIGURE 2 illustrates the drain characteristics of a particular unit. Other units of this geometry may be fabricated which may be used with higher negative gate voltages and/or with positive gate voltages. The maximum usable gate voltage is believed to be approximately ± 100 volts for the units of the type illustrated in FIGURE 1 and is limited by the dielectric breakdown strength of the converted layer 25, which is approximately 5×10^6 volts/cm.

FIGURE 3 illustrates a group of field-effect transistors having a ladder geometry. The ladder geometry facilitates the interconnection of many devices on a single semiconductor base or body. In the embodiment of FIGURE 3, the channel 27a is rectangular

and is approximately 0.0005 inch long and is approximately 0.05 inch wide. The length of channel 27a is defined as the dimension between the source and drain connections. The width is defined as the dimension perpendicular to the length and parallel to the top surface of the body 23a. The insulating layer 25a is of silicon oxide approximately 2700 Å thick which was converted from a single crystal body of high resistivity silicon. The deposited insulating layer portions 47 are of deposited silicon dioxide approximately one micron thick. The round tabs 45 at the ends of the gate electrodes 29a permit simple connection thereto with a thermally-bonded wire. Adjacent gate electrodes 29a are spaced on approximately 0.010 inch centres. The source electrode 35a of one transistor may function also as the drain electrode for an adjacent transistor. Also, the drain electrode 37a of one transistor may function as the source electrode for an adjacent transistor.

The group of field-effect transistors illustrated in FIGURE 3 may be fabricated by the method illustrated in FIGURES 4A, 4B and 4C: The single crystal wafer body 23a is of P-type silicon having a high resistivity of, for example, 500 ohm-cm. A surface of the wafer is cleaned to expose the body material. This may be achieved, for example, by etching the surface of the wafer with a chemical etchant to remove all of the disturbed material on the surface. Next, heavily doped silicon dioxide is deposited as a layer portion 47 on selected areas of the clean surface of the body 23a. For example, this is preferably achieved by depositing a uniform layer of doped silicon dioxide, as by thermal deposition from a doped oxy-silane, and then selectively removing the deposited oxide, as by selective etching using a photoresist technique.

The thickness of the deposited oxide is preferably between approximately 1 and 10 microns. The deposited oxide layer portions 47 contain a relatively high concentration of impurities (also referred to as a dopant) which are N-type when present in silicon. Such impurities are for example, antimony, arsenic, or phosphorus. The wafer is now heated at approximately 950°C in dry oxygen for approximately one hour and then cooled. During the heating, the surface portions of the silicon wafer 23a which are not covered with the deposited silicon dioxide layer 47 are converted to silicon dioxide 25a. Such converted material is sometimes referred to as thermally grown silicon dioxide. The converted material is essentially pure silicon dioxide and has a high resistivity approximately 10^{18} ohm-cm. A channel of low resistivity N-type material 27a forms between the layer 25a of silicon oxide and the bulk of the body 23a. The portion of the wafer which now includes the converted material 25a and the

channel 27a is referred to herein as a "reacted region".

During the same heating step, impurities from the deposited oxide layer portions 47 diffuse into the silicon under the deposited oxide layer portions 47 to form diffused regions 31a and 33a, in which the impurities decrease in concentration with the distance from the deposited layer portions 47. At the point of connection to the channel 27a and above, the diffused regions 31a and 33a have a relatively low resistivity.

Apertures are now etched through the deposited oxide layer portions 47 permitting access to a central part of the diffused regions 31a and 33a. This may be achieved by applying a photoresist to selected areas of the deposited and of the thermally grown silicon oxide layers 47 and 25a, respectively and then etching away portions where the holes are desired. Then, metal, such as aluminium, is selectively deposited on central parts of the diffused regions 31a and 33a, where the apertures were previously etched, and on the layer 25a of converted body material opposite to the channel 27a to form the source, drain, and gate electrodes 35a, 37a and 29a respectively. This may be accomplished by depositing, as by vapour deposition, a uniform layer of metal, such as aluminium, and then selectively removing the deposited metal using a photoresist technique leaving a source electrode 35a, a gate electrode 29a and a drain electrode 37a.

Ordinarily, the gate electrode 29a is co-extensive with the layer 25a of converted body material. However, this construction presents some fabrication difficulties, especially in aligning the gate electrode 29a over the layer of converted body material 25a. As illustrated in FIGURE 4C the gate electrode 29a is made longer than the channel 27a to extend over the parts of the deposited layer portions 47. The gate electrode 29a covers the entire layer 25a of converted material and parts of the deposited oxide layer portions 47. In this respect, FIGURE 4C differs from FIGURE 3 and therefore provides the third embodiment of the invention. The extended portions of the gate electrode 29a are indicated by the numeral 49. Since the thickness of the deposited oxide layer 47 is at least four times that of the layer 25a of converted material, this results in only a small amount of additional capacitance.

FIGURE 5 is a family of curves illustrating the drain characteristics (I_d plotted against V_d for different gate voltages, V_g) of the embodiment of FIGURE 4C. The transconductance is approximately 3,000 micromhos and the input capacitance measured at zero gate bias is fifteen picofarad, at approximately one mc (megacycle). When the channel 27a is completely depleted of free electrons by an applied gate voltage, the channel resist-

ance is approximately 20,000 ohms. This resistance is believed to be due to a parallel leakage path between the source and drain connections 31a and 33a around the gate electrode 29a.

The embodiment of FIGURE 4C may be operated at both positive and negative gate voltages V_g , as well as with no applied gate voltage. There is substantially no DC gate current flow at zero, positive or negative gate voltages. The upward turn of the curves for negative gate voltages at higher drain voltage is the effect of avalanche breakdown in the carrier depleted channel 27a. For example, the curve $V_g=3$ volts turns upward for values of V_d greater than approximately +10 volts. Gate current flow does not accompany this phenomenon.

The choice of material 23 for the base or body is important. The base may be any single crystal or polycrystalline semiconductor material which may be used to prepare semiconductor devices. The base material should preferably have a high resistivity and be capable of producing an insulating layer of high resistivity by chemical conversion of a region of the body. The preferred base material is single crystal silicon. With low resistivity P-type silicon as the base material only partial compensation may occur in the channel region and an N-type layer may not be obtained when the converted layer is produced. P-type silicon, typically between 2 and 1000 ohm-cm resistivity, is a preferred base material. Generally, in P-type silicon, the higher the resistivity of the base, the greater the number of free N-type charge carriers in the channel. If a P-type channel is desired between the bulk of the base and the layer of converted body material, then high resistivity N-type silicon should be used as the base.

The drain characteristics of the embodiment of FIGURE 4C may also be modified by changing the time of heating in the range between 0.5 and 40 hours and/or the temperature in the range between 850° and 1100°C to produce the converted layer. The longer heating times and higher heating temperatures converts the silicon of the body to a greater depth, and produces a channel of greater depth.

FIGURE 6 is a family of curves of an embodiment similar in geometry to that illustrated in FIGURE 4C except that the heating step was continued for approximately two hours at approximately 950°C in dry oxygen. This produced a thicker reacted region including a deeper channel. Also, depending on the atmosphere and on the surface treatment prior to oxidation, either a P-type or a N-type channel (inversion layer) may be formed. Either type of channel is operative. However, the connections to the channel should be of the same conductivity type as

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that of the channel. Where P-type source and drain connections are desired for silicon, the deposited oxide layer should contain P-type impurities for silicon such as indium or boron. Where N-type source and drain connections are desired for silicon, the deposited oxide layer should contain N-type impurities for silicon, such as arsenic, antimony, or phosphorus.

It has been found that baking the base for one or more hours in a dry inert atmosphere after the formation of the converted layer reduces the number of free charge carriers present in the channel. For instance, in the device of FIGURE 4C, the concentration of free charge carriers in the channel 27a produced during the heating step can be reduced by subsequently baking the silicon wafer at approximately 1000°C for approximately one hour in dry nitrogen. The overall method is the same as that described above with respect to fabricating the device of FIGURE 4C, except that before the electrodes are applied, the assembly is heated in an inert atmosphere and then cooled.

FIGURE 7 is a family of curves illustrating the drain characteristic of a field-effect transistor prepared by this modified method. The transistor is referred to as an enhancement field-effect transistor because the principal mode of operation is by the further enhancement to the channel of free charge carriers in response to a positive gate voltage, for an N-type channel.

The structure of FIGURE 8 is similar to that of FIGURE 3 except that adjacent gate electrodes 29b are connected at both ends so that the drain electrode 37b of each unit is completely surrounded by a modified gate electrode. As illustrated in FIGURE 8, each unit is comprised of two source electrodes 35b and one drain electrode 37b enclosed by the gate electrode 29b. In this embodiment, the drain electrode of one unit is not intended to function as a source electrode for an adjacent unit.

FIGURE 9 is a family of curves illustrating the drain characteristics of the unipolar field-effect transistor illustrated in FIGURE 8. The device may be operated in either the depletion mode (negative gate voltage) or the enhancement mode (positive gate voltage). The transistor having the modified gate electrode arrangement of FIGURE 8 has a lower leakage current than the transistor of FIGURE 3 having the ladder geometry. This results from the fact that the drain electrode is completely surrounded by the gate electrode.

It is clear that the illustrated transistor devices and their methods of preparation are particularly advantageous in integrated circuits since the devices may be prepared simultaneously in large numbers on a single wafer. It should be noted that the devices

may be prepared using only one surface of the wafer.

WHAT WE CLAIM IS:—

1. A field-effect transistor comprising a substrate of semiconductor material of one conductivity type, a low resistivity channel of semiconductor material of the opposite conductivity type in said substrate, said channel being substantially free of dopants of said opposite conductivity type, a source of semiconductor material of said opposite conductivity type in said substrate contacting said channel, a drain of semiconductor material of said opposite conductivity type in said substrate contacting said channel, and a gate electrode opposite to and spaced from said channel by an insulating layer of high resistivity material.

2. A transistor according to Claim 1 having first and second electrodes respectively connected to said source and said drain, and wherein said insulating layer is formed of converted substrate material, such as an oxide of said substrate material.

3. A transistor according to Claim 2, wherein said gate electrode extends over and is spaced from a portion of said source and a portion of said drain the spacing between said gate electrode and said channel being substantially smaller than each of the spacings between said gate electrode and said source and said gate electrode and said drain.

4. A transistor according to Claim 2 or Claim 3, wherein said substrate is P-type silicon, said layer of converted substrate material is silicon oxide, and said low resistivity channel is N-type silicon.

5. A transistor according to Claim 2 or Claim 3, wherein said substrate is P-type silicon, said source includes a first low resistivity impurity diffused region of N-type silicon in said substrate which contacts and defines one end of said channel, and said drain includes a second low resistivity impurity diffused region of N-type silicon in said substrate which contacts and defines the other end of said channel.

6. A transistor according to Claim 3, wherein a first layer of silicon oxide is arranged on a portion of said source and abuts said layer of converted substrate material, a second layer of silicon oxide is arranged on a portion of said drain and abuts said layer of converted substrate material, said first and second layers being thicker than said layer of converted material, and wherein said gate electrode extends over at least a part of said second deposited layer.

7. An electrical circuit comprising a plurality of transistors according to Claim 1, wherein said substrate of semiconductor material includes a plurality of layers of converted substrate material such as oxides of said substrate material, each layer being respectively separated from the bulk of said

that of the channel. Where P-type source and drain connections are desired for silicon, the deposited oxide layer should contain P-type impurities for silicon such as indium or boron. Where N-type source and drain connections are desired for silicon, the deposited oxide layer should contain N-type impurities for silicon, such as arsenic, antimony, or phosphorus.

It has been found that baking the base for one or more hours in a dry inert atmosphere after the formation of the converted layer reduces the number of free charge carriers present in the channel. For instance, in the device of FIGURE 4C, the concentration of free charge carriers in the channel 27a produced during the heating step can be reduced by subsequently baking the silicon wafer at approximately 1000°C for approximately one hour in dry nitrogen. The overall method is the same as that described above with respect to fabricating the device of FIGURE 4C, except that before the electrodes are applied, the assembly is heated in an inert atmosphere and then cooled.

FIGURE 7 is a family of curves illustrating the drain characteristic of a field-effect transistor prepared by this modified method. The transistor is referred to as an enhancement field-effect transistor because the principal mode of operation is by the further enhancement to the channel of free charge carriers in response to a positive gate voltage, for an N-type channel.

The structure of FIGURE 8 is similar to that of FIGURE 3 except that adjacent gate electrodes 29b are connected at both ends so that the drain electrode 37b of each unit is completely surrounded by a modified gate electrode. As illustrated in FIGURE 8, each unit is comprised of two source electrodes 35b and one drain electrode 37b enclosed by the gate electrode 29b. In this embodiment, the drain electrode of one unit is not intended to function as a source electrode for an adjacent unit.

FIGURE 9 is a family of curves illustrating the drain characteristics of the unipolar field-effect transistor illustrated in FIGURE 8. The device may be operated in either the depletion mode (negative gate voltage) or the enhancement mode (positive gate voltage). The transistor having the modified gate electrode arrangement of FIGURE 8 has a lower leakage current than the transistor of FIGURE 3 having the ladder geometry. This results from the fact that the drain electrode is completely surrounded by the gate electrode.

It is clear that the illustrated transistor devices and their methods of preparation are particularly advantageous in integrated circuits since the devices may be prepared simultaneously in large numbers on a single wafer. It should be noted that the devices

may be prepared using only one surface of the wafer.

WHAT WE CLAIM IS:—

1. A field-effect transistor comprising a substrate of semiconductor material of one conductivity type, a low resistivity channel of semiconductor material of the opposite conductivity type in said substrate, said channel being substantially free of dopants of said opposite conductivity type, a source of semiconductor material of said opposite conductivity type in said substrate contacting said channel, a drain of semiconductor material of said opposite conductivity type in said substrate contacting said channel, and a gate electrode opposite to and spaced from said channel by an insulating layer of high resistivity material.

2. A transistor according to Claim 1 having first and second electrodes respectively connected to said source and said drain, and wherein said insulating layer is formed of converted substrate material, such as an oxide of said substrate material.

3. A transistor according to Claim 2, wherein said gate electrode extends over and is spaced from a portion of said source and a portion of said drain the spacing between said gate electrode and said channel being substantially smaller than each of the spacings between said gate electrode and said source and said gate electrode and said drain.

4. A transistor according to Claim 2 or Claim 3, wherein said substrate is P-type silicon, said layer of converted substrate material is silicon oxide, and said low resistivity channel is N-type silicon.

5. A transistor according to Claim 2 or Claim 3, wherein said substrate is P-type silicon, said source includes a first low resistivity impurity diffused region of N-type silicon in said substrate which contacts and defines one end of said channel, and said drain includes a second low resistivity impurity diffused region of N-type silicon in said substrate which contacts and defines the other end of said channel.

6. A transistor according to Claim 3, wherein a first layer of silicon oxide is arranged on a portion of said source and abuts said layer of converted substrate material, a second layer of silicon oxide is arranged on a portion of said drain and abuts said layer of converted substrate material, said first and second layers being thicker than said layer of converted material, and wherein said gate electrode extends over at least a part of said second deposited layer.

7. An electrical circuit comprising a plurality of transistors according to Claim 1, wherein said substrate of semiconductor material includes a plurality of layers of converted substrate material such as oxides of said substrate material, each layer being respectively separated from the bulk of said



- substrate by a different low resistivity channel, a plurality of sources and drains, each of said sources and drains except for the end ones being respectively connected to two different channels and acting as a source for one channel and a drain for the other of said two different channels, and a plurality of gate electrodes, each of said gate electrodes being arranged upon a respectively different one of said plurality of layers and being spaced from said one layer's respective low resistivity channel.
8. A method of fabricating a field-effect transistor comprising the steps of: producing at least two spaced insulating layer portions on a surface of a semiconductor substrate of high resistivity material and having one conductivity type, said layer portions containing impurities of opposite conductivity type to said substrate, producing a reacted region in said substrate between said insulating layer portions, said reacted region including a converted layer of the substrate material, such as an oxide of said substrate, and a low resistivity channel between the bulk of said body and said converted layer of substrate material, causing said impurities to diffuse from said layer portions into said substrate to form low resistivity diffused regions contiguous with and defining the ends of said channel, and then producing an electrode on said converted layer of substrate material opposite to and spaced from said channel.
9. A method according to Claim 8 and comprising depositing a layer of silicon dioxide on a surface of silicon semiconductor substrate, to produce said two spaced insulating layer portions said one conductivity type of impurity in said layer being N-type impurity for said body, and selectively removing material from said deposited silicon dioxide layer to leave said two spaced layer portions on said substrate.
10. A method according to Claim 9 and comprising the step of heating said substrate in an oxidizing atmosphere simultaneously to convert said substrate material and to cause said impurities to diffuse from said layer portions into said substrate.
11. A method according to Claim 10, wherein said heating step is carried out at a temperature of between 850° to 1100°C.
12. A method according to Claim 11, wherein said heating step has a duration of between 0.5 to 40 hours and comprising the steps of selectively removing material from each of said deposited layer portions so as to expose each of said diffused regions in said substrate and depositing metal contacts on to each of said diffusing regions.
13. A method in accordance with any one of Claims 10, 11 and 12, wherein said semiconductor substrate is high resistivity silicon material.
14. A field-effect transistor when made by a method according to any one of Claims 8 to 13.
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