

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
4 September 2003 (04.09.2003)

PCT

(10) International Publication Number
WO 03/073428 A1

(51) International Patent Classification⁷: **G11C 11/34**,
11/56

(21) International Application Number: PCT/US03/03226

(22) International Filing Date: 5 February 2003 (05.02.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/081,594 20 February 2002 (20.02.2002) US

(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 S. Federal Way, Boise, ID 83707-0006 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

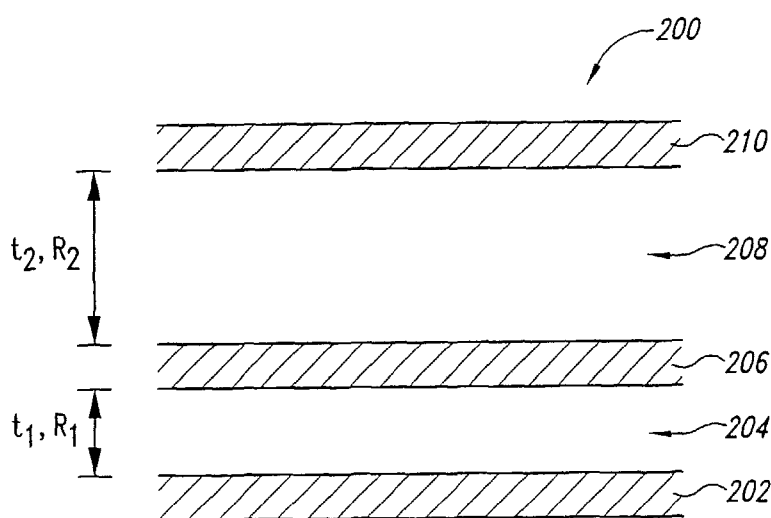
(72) Inventor: **GILTON, Terry, L.**; 3149 East Nature Drive,
Boise, ID 83706 (US).

Published:
— with international search report

(74) Agent: **D'AMICO, Thomas, J.**; Dickstein Shapiro Morin
& Oshinsky LLP, 2101 L Street NW, Washington, DC
20037-1526 (US).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MULTIPLE DATA STATE MEMORY CELL



(57) Abstract: A programmable multiple data state memory cell including a first electrode layer formed from a first conductive material, a second electrode layer formed from a second conductive material, and a first layer of a metal-doped chalcogenide material disposed between the first and second electrode layers. The first layer providing a medium in which a conductive growth can be formed to electrically couple together the first and second electrode layers. The memory cell further includes a third electrode layer formed from a third conductive material, and a second layer of a metal-doped chalcogenide material disposed between the second and third electrode layers, the second layer providing a medium in which a conductive growth can be formed to electrically couple together the second and third electrode layers.

WO 03/073428 A1