Figure 1

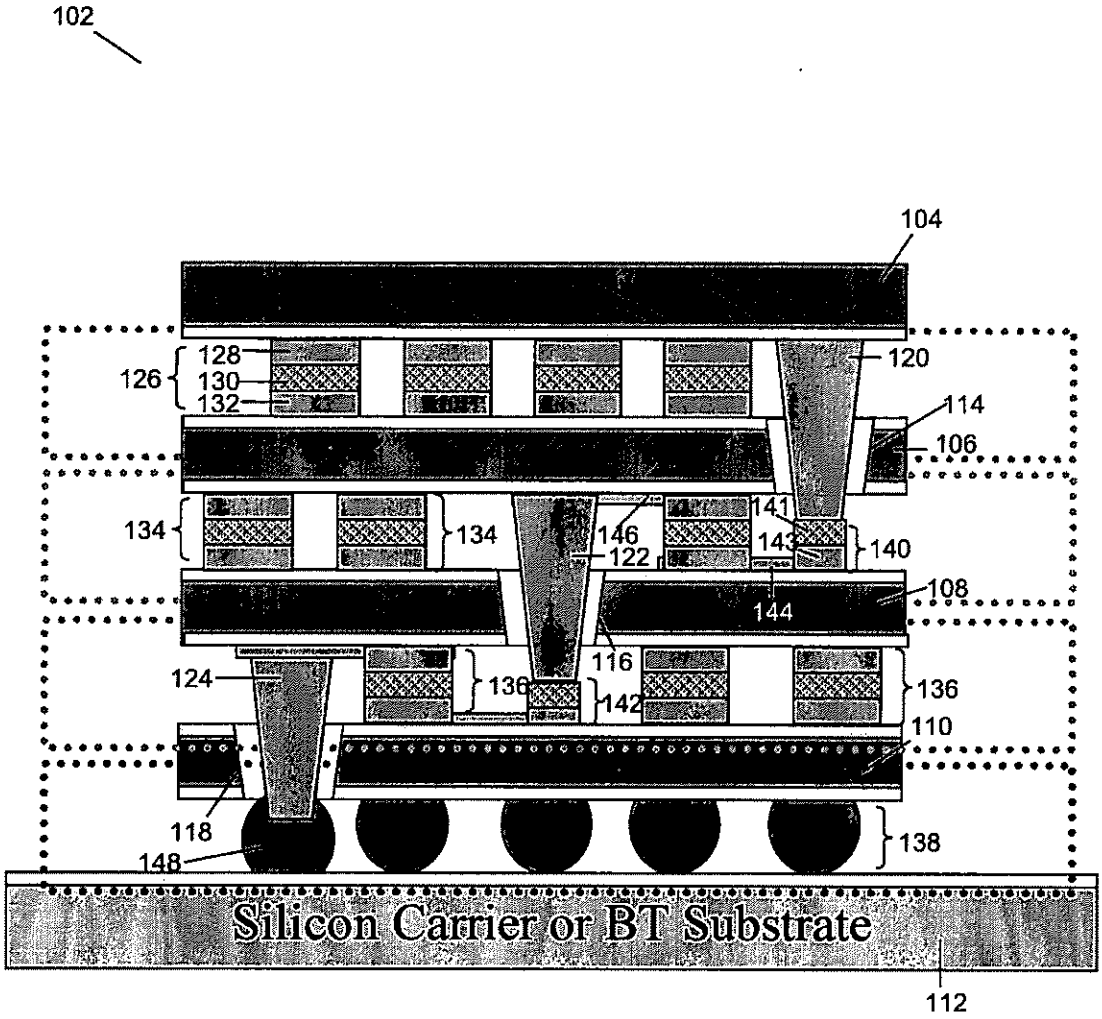

102
104
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148
138
Silicon Carrier or BT Substrate
112

Figure 2

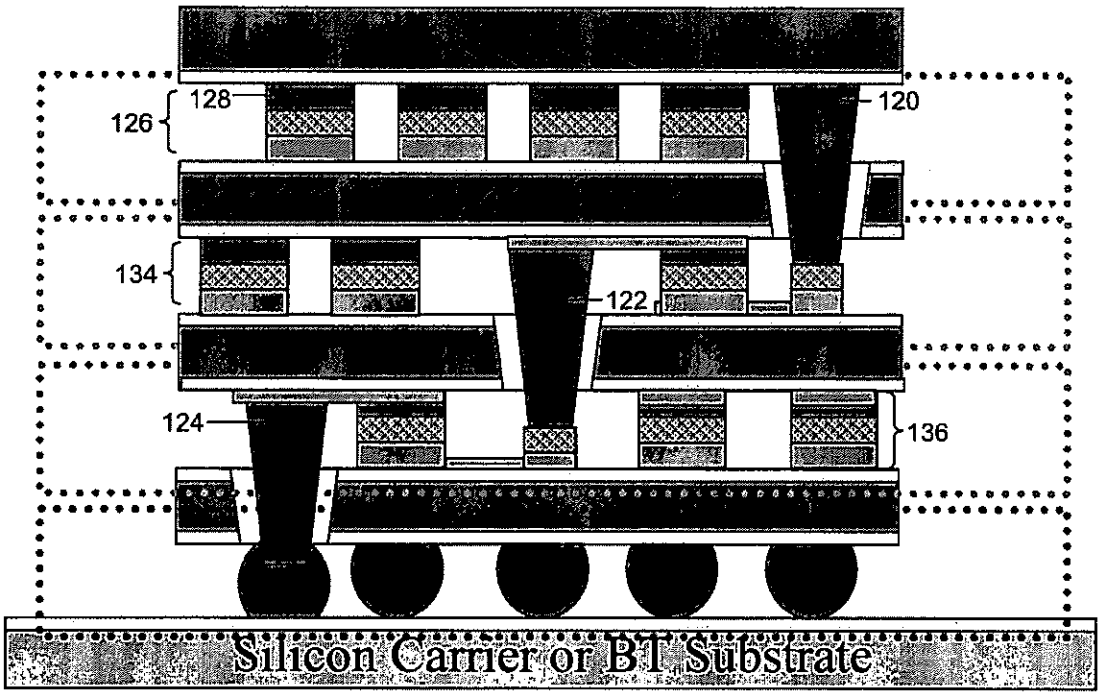


Figure 3

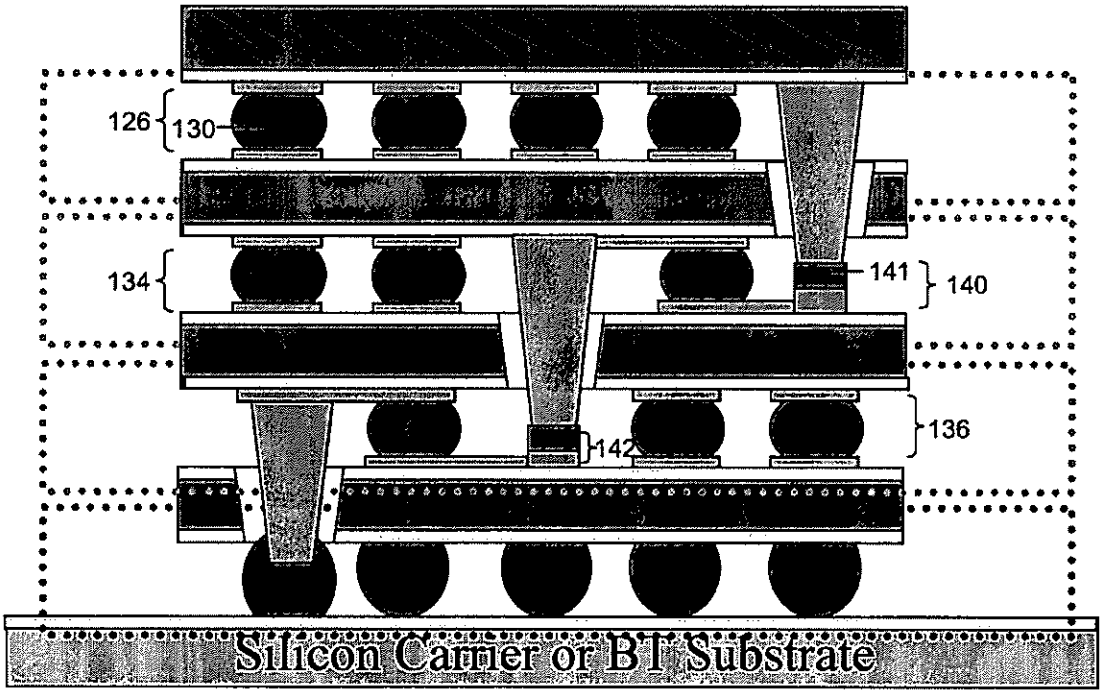


Figure 4A

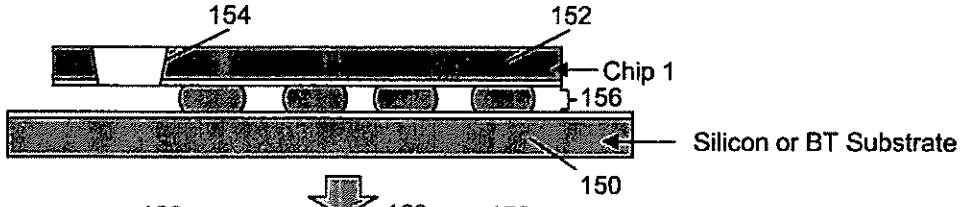


Figure 4B

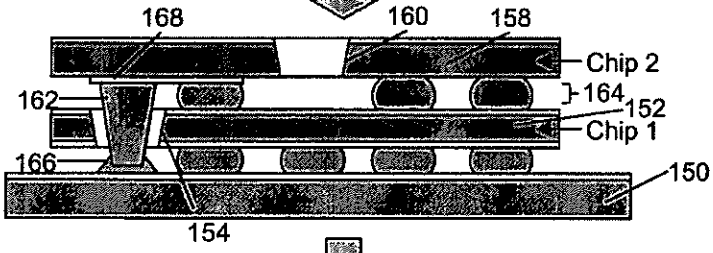


Figure 4C

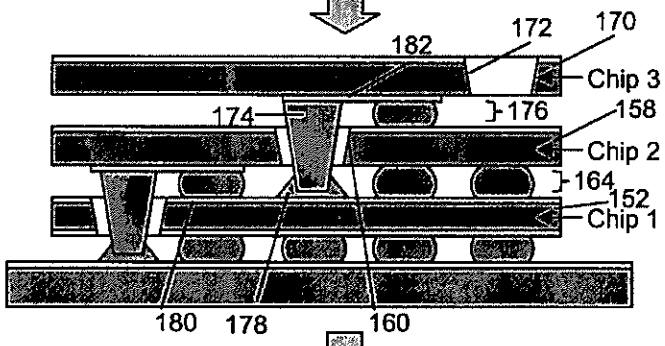


Figure 4D

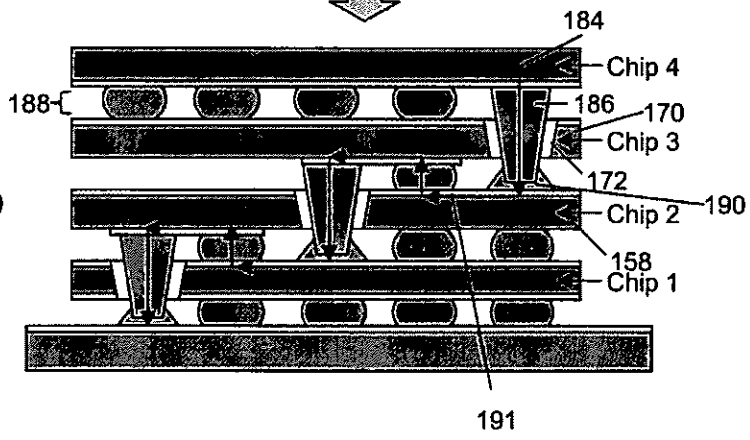


Figure 5A

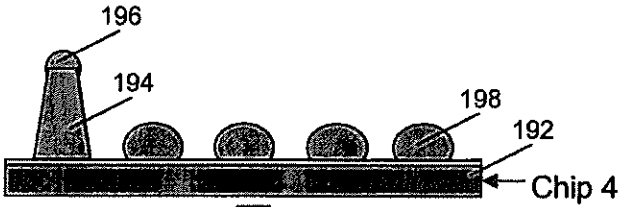


Figure 5B

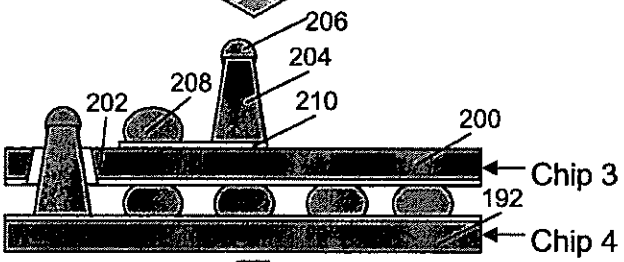


Figure 5C

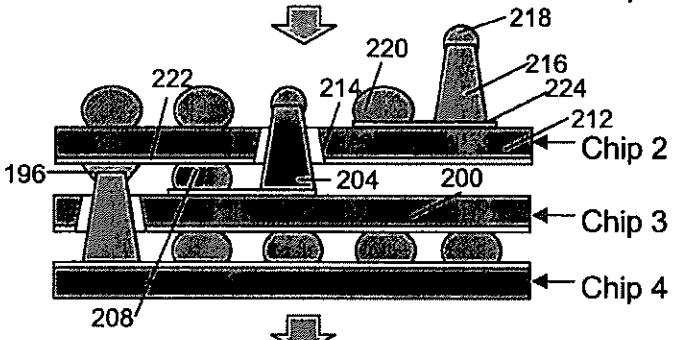


Figure 5D

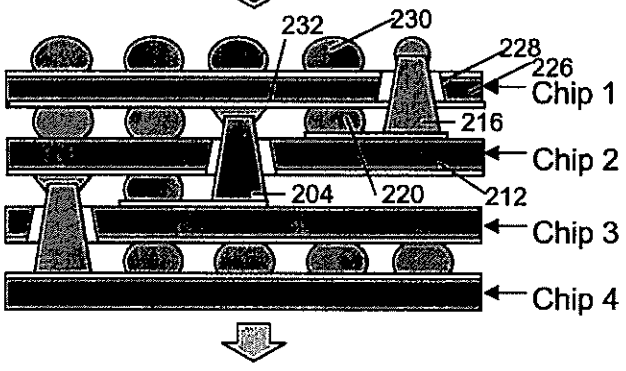


Figure 5E

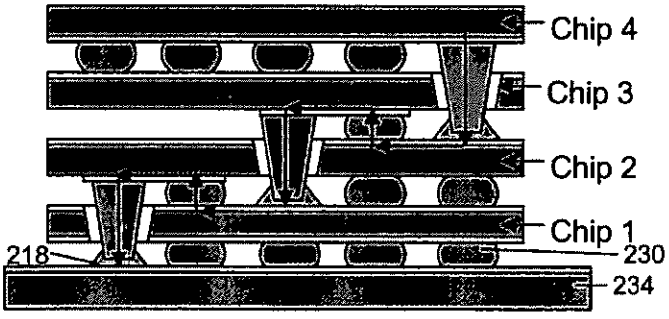


Figure 6A

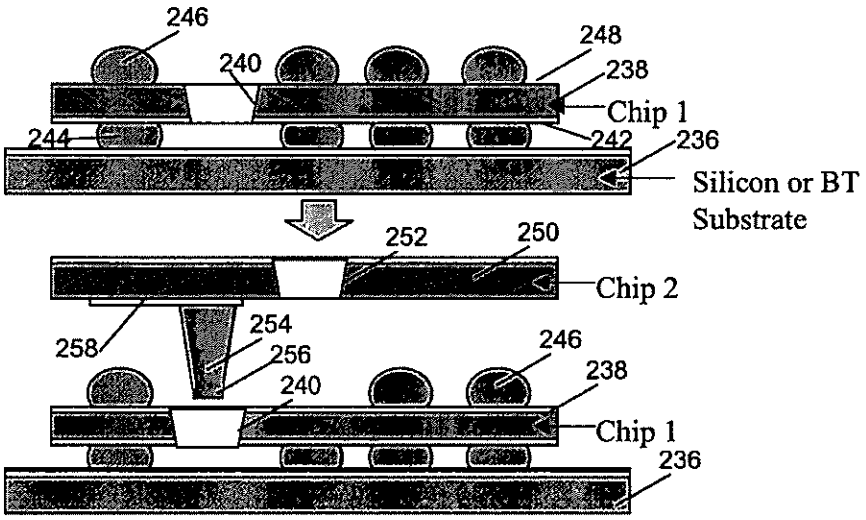


Figure 6B

Chip with double side bump

Figure 7A

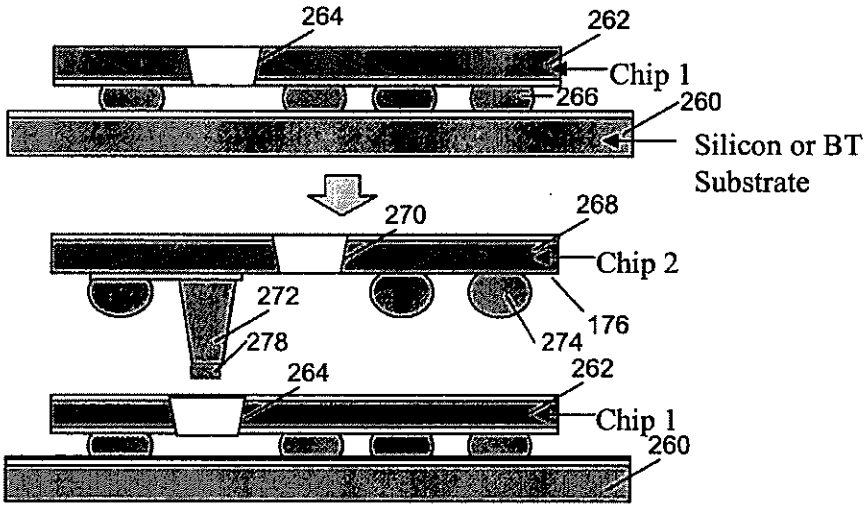


Figure 7B

Chip with Bump and Copper pillar on the active side

Figure 8A

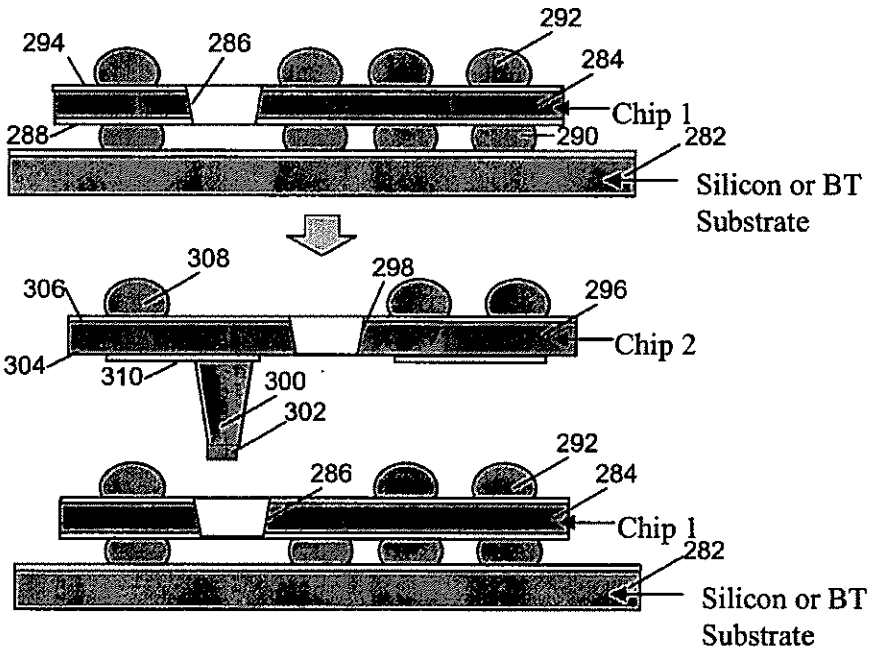


Figure 8B

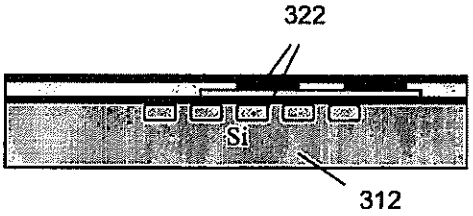
Chip with Copper pillar on the active side and Bump on the passive side

Figure 9A



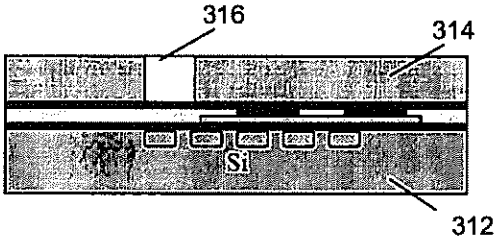
Starting substrate — 902

Figure 9B



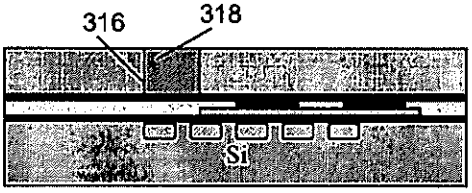
Forming Circuits on Top side of substrate/wafer — 904

Figure 9C



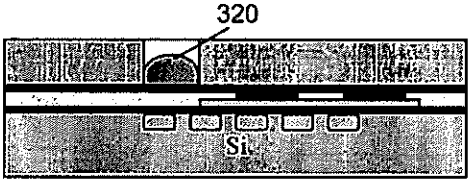
Deposit and Pattern Photoresist — 906

Figure 9D



Solder plating or screen printing — 908

Figure 9E



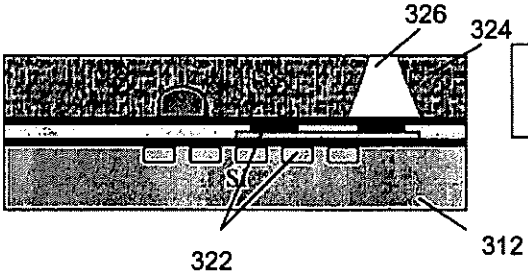
Reflow — 910

Figure 9F



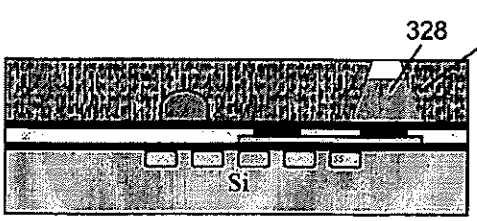
Strip Photoresist — 912

Figure 9G



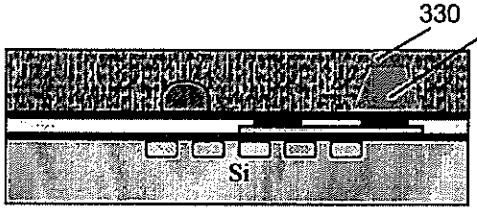
Laminated and Patterned Photosensitive layer — 914

Figure 9H



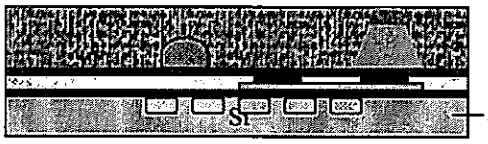
Cu Column plating — 916

Figure 9I



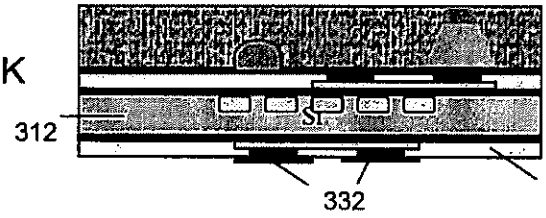
Solder plating or screen printing — 918

Figure 9J



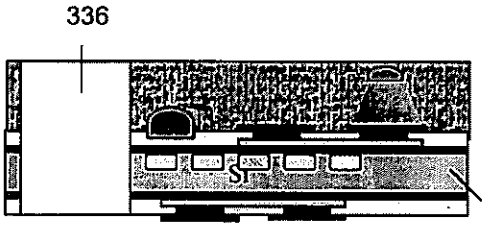
Backgrind substrate/wafer — 920

Figure 9K



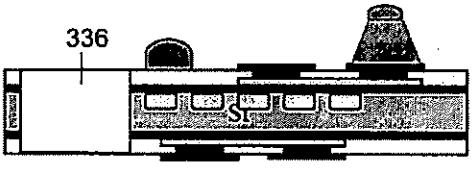
Metallization and passivation (parylene/paralene) process — 922

Figure 9L



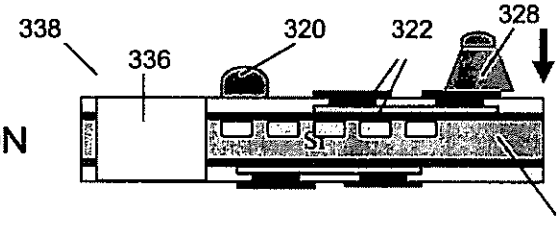
Laser drill or low temperature DRIE — 924

Figure 9M



Photosensitive stripping & Reflow — 926

Figure 9N



Laser /Mechanical dicing — 928

Figure 10A



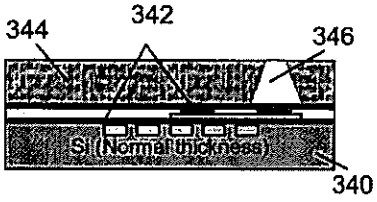
Starting substrate — 1002

Figure 10B



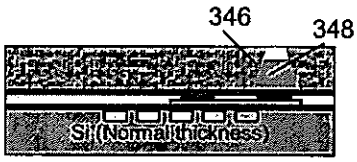
Forming Circuits on Top side of wafer — 1004

Figure 10C



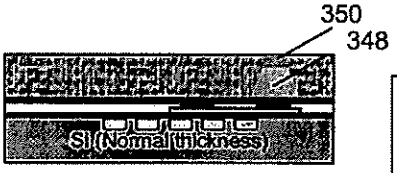
Laminated and Patterned Photosensitive layer — 1006

Figure 10D



Cu Column plating — 1008

Figure 10E



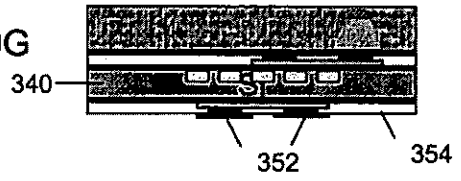
Solder plating or screen printing — 1010

Figure 10F



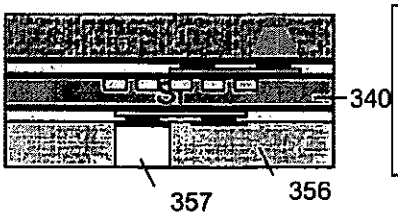
Backgrind wafer — 1012

Figure 10G



Metallization and passivation (parylene/paralene) process — 1014

Figure 10H



Deposit and Pattern Photoresist — 1016

Figure 10I

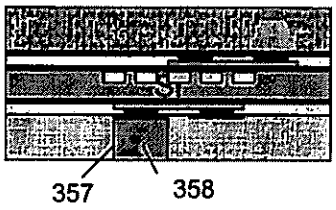


Figure 10J

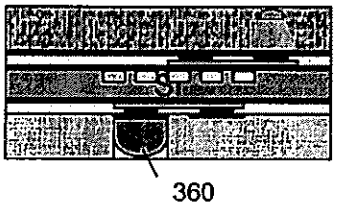


Figure 10K

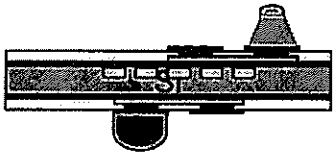


Figure 10L

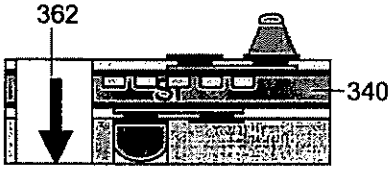


Figure 10M

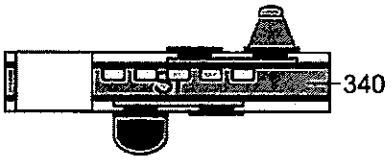
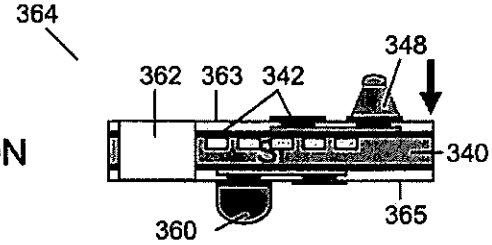


Figure 10N



Solder plating or screen printing — 1018

Reflow — 1020

Strip Photosensitive layer — 1022

Laser Drill or Low Temperature DRIE — 1024

Strip Photoresist — 1026

Laser /Mechanical Dicing — 1028

Figure 11

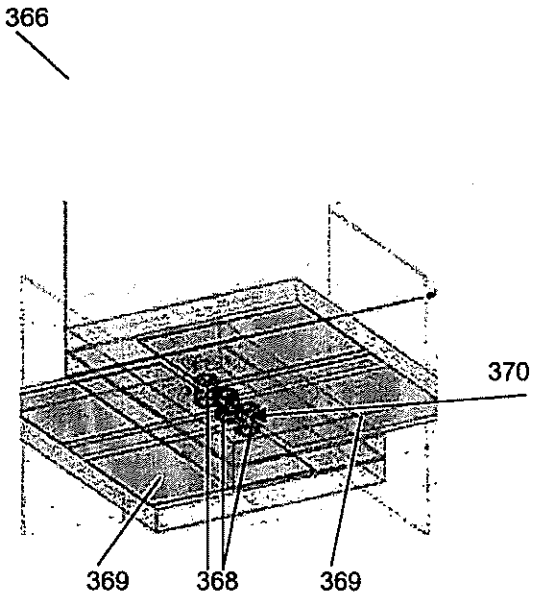
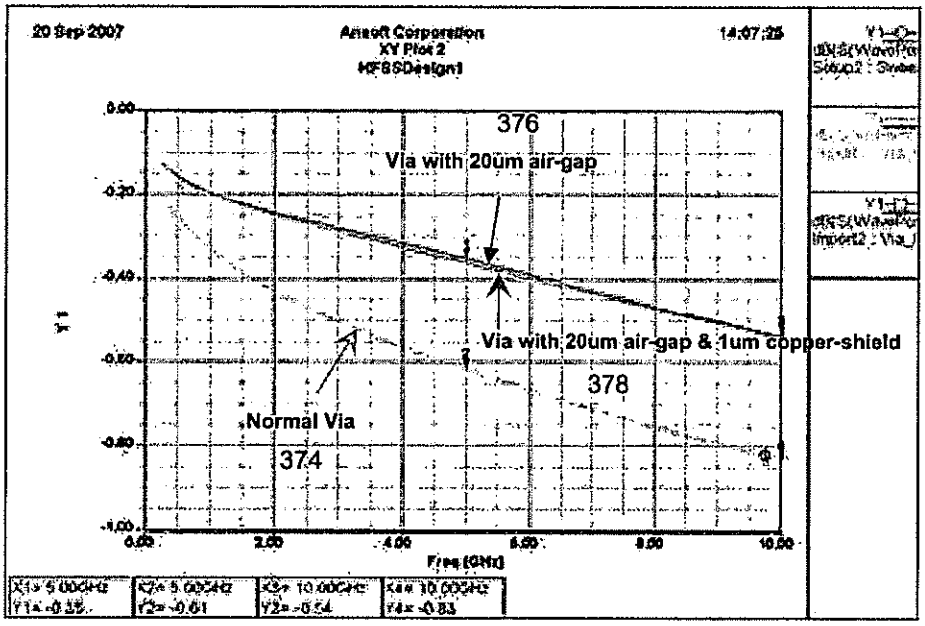

366
370
Via with air gap. Cu column are then inserted into these through vias which do not touch the sides of the vias
369
368
369

Figure 12


20 Sep 2007
Ansoft Corporation
XY Plot 2
HFSSDesign1
14:07:25
376
Via with 20um air-gap
Via with 20um air-gap & 1um copper-shield
378
Normal Via
374
Freq [GHz]

71.907 MPa

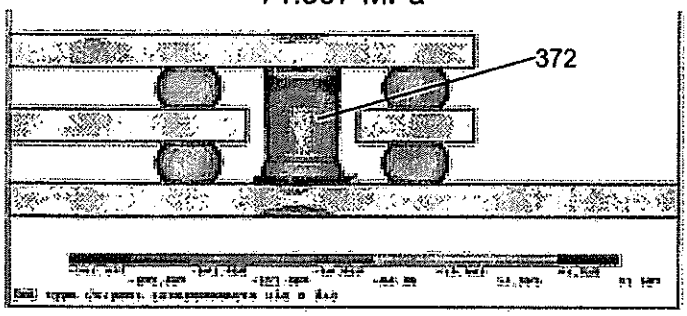


Figure 13A

364.49 MPa

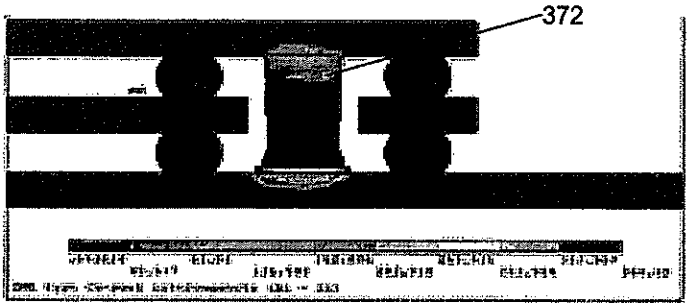


Figure 13B

386.175 MPa

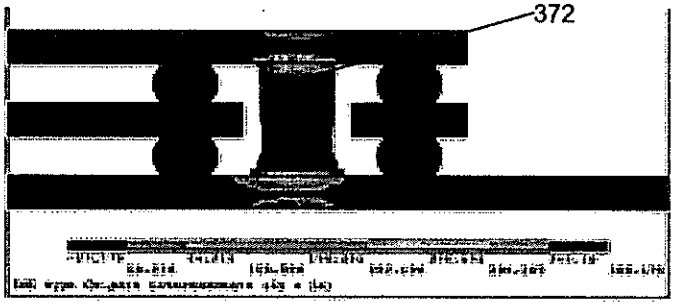


Figure 13C