SEMICONDUCTOR STRUCTURE AND METHOD OF FABRICATING THE SAME

FIELD OF INVENTION

The invention relates to a semiconductor structure and a method of fabricating the same.

BACKGROUND

The emergence of electronic devices such as smart-phones, tablets and portable computers has resulted in an increase in demand for high performance integrated circuits (ICs). These electronic devices are continually moving toward higher functionality and size miniaturization. In order to keep up with this trend, IC packages are becoming smaller, thinner and more compact.

It is possible to reduce the size and thickness of IC packages by increasing wiring density and reducing the thickness of substrates used in IC packages. However, as substrate thickness is reduced, the substrate becomes more prone to damage (such as cracks or dents) during handling and subsequent assembly process steps. This is especially prevalent when the material used for the substrate has a high flexural modulus (in order to achieve a low coefficient of thermal expansion (CTE)). This is more apparent as the size of the substrate increases to accommodate more device units on each substrate in order to reduce manufacturing cost.

A need therefore exists to provide a semiconductor structure and a method of fabricating the same that seeks to address at least one of the abovementioned problems.

SUMMARY

According to the first aspect of the invention, there is provided a semiconductor structure, comprising: a discontinuous layer element comprising two or more discrete sections; one or more supporting elements disposed on a first surface of the layer element wherein one supporting element is disposed across each gap between adjacent discrete sections of the layer element, and two or more anchoring elements disposed within the layer element and connected to the one or more supporting elements to couple the one or more supporting elements to the layer element to strengthen the layer element, wherein each of the two or more anchoring elements comprises an upper section and a lower section, wherein, relative to the lower section, the upper section has a larger cross-sectional area in a plane parallel to the first surface of the layer element, the upper section being connected to the one or more supporting elements.

elements of the layer element to strengthen both the layer element and the further layer element.

According to the second aspect of the invention, there is provided method of fabricating a semiconductor structure, the method comprising: forming two or more anchoring elements over a carrier such that each of the two or more anchoring elements comprises an upper section and a lower section, and such that, relative to the lower section, the upper section has a larger cross-sectional area in a plane parallel to the first surface of the layer element; encapsulating the two or more anchoring elements within a discontinuous layer element comprising two or more discrete sections; and selectively etching the carrier to form one or more supporting elements such that the one or more supporting elements are connected to the upper section of the respective two or more anchoring elements and one supporting element is disposed across each gap between adjacent discrete sections of the layer element.

In an embodiment, the method may further comprise forming one or more electrical elements over the carrier.

In an embodiment, the method may further comprise forming one or more through-holes in the one or more supporting elements.

In an embodiment, the method may further comprise planarizing the layer element to expose at least a portion of at least one of the one or more anchoring elements.

In an embodiment, the method may further comprise forming one or more reinforcement elements over at least a portion of the one or more exposed anchoring elements.

In an embodiment, the method may further comprise forming one or more reinforcement elements over at least a portion of the one or more supporting elements.

In an embodiment, the method may further comprise forming a coating over at least a portion of an inner magnetic core; the inner magnetic core and coating defining the carrier.

In an embodiment, the method may further comprise forming one or more dividing gaps in the layer element.

Fig. 11 is a cross-section view of a semiconductor structure, according to another embodiment of the invention.

Fig. 12a – d are cross-section views of a semiconductor structure, according to embodiments of the invention.

Fig. 13a and b is a bottom and enlarged view, respectively, of a semiconductor structure, according to an embodiment of the invention.

Fig. 14 is a cross-section view of a semiconductor structure, according to another embodiment of the invention.

Fig. 15a and b is a top and bottom view, respectively, of a semiconductor structure, according to an embodiment of the invention.

Figs. 16 a – f are cross-section diagrams illustrating the fabrication process of semiconductor structures, according to an embodiment of the invention.

Figs. 17 a – e are cross-section diagrams illustrating the fabrication process of semiconductor structures, according to an embodiment of the invention.

Figure 18 is a flow chart illustrating the steps of a method of fabricating a semiconductor structure, according to an embodiment of the invention.

DETAILED DESCRIPTION

Embodiments of the present invention will be described with reference to the drawings. Like reference numerals and characters in the drawings refer to like elements or equivalents.

Fig. 1 is a schematic of a semiconductor structure, designated generally as reference numeral 100, according to an embodiment of the present invention. The semiconductor structure 100 comprises a layer element 102; two supporting (stiffening) elements 104a / 104b disposed on a first surface of the layer element 102; and two anchoring (locking) elements 106a / 106b disposed within the layer element 102, and connected to the two supporting elements 104a / 104b, respectively. The two anchoring elements 106a / 106b are connected to the two

CLAIMS

1. A semiconductor structure, comprising:

a discontinuous layer element comprising two or more discrete sections;

one or more supporting elements disposed on a first surface of the layer element wherein one supporting element is disposed across each gap between adjacent discrete sections of the layer element, and

two or more anchoring elements disposed within the layer element and connected to the one or more supporting elements to couple the one or more supporting elements to the layer element to strengthen the layer element,

wherein each of the two or more anchoring elements comprises an upper section and a lower section,

wherein, relative to the lower section, the upper section has a larger cross-sectional area in a plane parallel to the first surface of the layer element, the upper section being connected to the one or more supporting elements.

2. The semiconductor structure as claimed in claim 1, wherein a portion of at least one of the two or more anchoring elements is exposed on a second surface of the layer element, the second surface being opposite the first surface.

3. The semiconductor structure as claimed in claim 2, further comprising one or more reinforcement elements disposed on at least a portion of the second surface of the layer element, wherein the two or more anchoring elements are connected to the one or more reinforcement elements to couple the one or more reinforcement elements to the layer element to further strengthen the layer element.

4. The semiconductor structure as claimed in claim 1, further comprising one or more reinforcement elements disposed on at least a portion of the one or more supporting elements to further strengthen the layer element.

5. The semiconductor structure as claimed in claim 1, wherein the one or more supporting elements comprise a magnetic material.

6. The semiconductor structure as claimed in claim 5, wherein the one or more supporting elements further comprise a coating, the coating being disposed over at least a portion of the magnetic material.

7. The semiconductor structure as claimed in claim 1, wherein the one or more supporting elements are disposed at an edge portion of the layer element.

8. The semiconductor structure as claimed claim 7, wherein a portion of the one or more supporting elements extend beyond the edge of the layer element to define an overhang portion.

9. The semiconductor structure as claimed in claim 8, wherein the overhang portion comprises one or more through-holes.

10. The semiconductor structure as claimed in claim 1, wherein the layer element comprises an insulating substrate layer element having one or more electrical elements.

11. The semiconductor structure as claimed in claim 1, comprising one supporting element, wherein the one supporting element extends around a perimeter of the layer element.

12. The semiconductor structure as claimed in claim 1, wherein at least one of the two or more anchoring elements is a pillar or column.

13. The semiconductor structure as claimed in claim 1, further comprising:

a further layer element; and

one or more further anchoring elements disposed within the further layer element and connected to the two or more anchoring elements of the layer element to strengthen both the layer element and the further layer element.

14. A method of fabricating a semiconductor structure, the method comprising:

forming two or more anchoring elements over a carrier such that each of the two or more anchoring elements comprises an upper section and a lower section, and such that, relative to the lower section, the upper section has a larger cross-sectional area in a plane parallel to the first surface of the layer element;

encapsulating the two or more anchoring elements within a discontinuous layer element comprising two or more discrete sections; and

selectively etching the carrier to form one or more supporting elements such that the one or more supporting elements are connected to the upper section of the respective two or more anchoring elements and one supporting element is disposed across each gap between adjacent discrete sections of the layer element.

15. The method as claimed in claim 14, further comprising forming one or more electrical elements over the carrier.

16. The method as claimed in claim 14, further comprising forming one or more through-holes in the one or more supporting elements.

17. The method as claimed in claim 14, further comprising planarizing the layer element to expose at least a portion of at least one of the two or more anchoring elements.

18. The method as claimed in claim 17, wherein planarizing the layer element comprises magnetically securing the carrier to a work plane.

19. The method as claimed in claim 18, wherein magnetically securing the carrier to a work plane comprises disposing the carrier comprising a magnetic material on the work plane comprising an electromagnet or permanent magnet.

20. The method as claimed in claim 17, further comprising forming one or more reinforcement elements over at least a portion of the two or more exposed anchoring elements.

21. The method as claimed in claim 14, further comprising forming one or more reinforcement elements over at least a portion of the one or more supporting elements.

22. The method as claimed in claim 14, further comprising forming a coating over at least a portion of an inner magnetic core; the inner magnetic core and coating defining the carrier.

23. The method as claimed in claims 14, further comprising forming one or more dividing gaps in the layer element.