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AREA ARRAY STUD BUMP FLIP CHIP DEVICE AND ASSEMBLY PROCESS

FIELD OF THE INVENTION

5 The present invention is related to flip chip technology. In particular, the present invention is related to the interconnection between an integrated circuit chip and its corresponding substrate in flip chip device production. This invention is also related to the interconnection between an integrated circuit device and second level substrate such as a printed circuit board or
10 card.

BACKGROUND OF THE INVENTION

An IC device is produced by electrically interconnecting an IC chip to an electronic substrate (hereinafter called substrate) to form one device. An electronic substrate is a non-conducting material containing single or
15 multilayer electrically conducting traces for electrical connection. Flip chip device is produced by mounting an integrated circuit (IC) chip onto a substrate in a manner such that the active area of the IC chip and the substrate faces each other, and are electrically interconnected. Compared to other conventional methods of mounting, such as face-up wire bonding
20 and face-up tape-automated bonding, flip chip technology provides the shortest possible leads, lowest inductance and highest frequency and density. *Flip Chip Technologies* edited by John H. Lau (1996) (Reference 1) gives an overview of the state of the art in this technology. In flip chip technology, the interconnection used to electrically connect the IC chip to

the substrate include wire bumping, and solder bumping. Solder bumping can be performed on the IC chip surface and are thus useful for area array designs while wire bumping is commonly used for interconnection at the periphery of the IC chip.

5 . Wire bonding involves the use of a wire bonder which has a wire fed through a tool called a capillary. The end of the wire is heated to a molten state where the surface tension of the liquid metal forms the shape of a ball. The capillary descends on the bond pad of the chip with a force to form a weld between the wire and the chip bond pad. Often, ultrasonic energy is
10 included in the bonding process, in which case the process is known as thermosonic bonding. Typically the wirebond pads are situated over the periphery of the IC chips. In some instances such as in a memory chip, the bond pads are designed to be situated over the mid region of the chip. In either case, the bond pads cannot be formed over the active area of the
15 chip.

Stud bumping is a modification of the wire bonding technique. Instead of a wire connection between the bonded IC chip and the I/O pad of the substrate, the wire is cut at the bonded ball, leaving behind a stud bump. Baba, S. in the IEEE 47th Electronic Components and Technology
20 Conference Proceedings in 1997 pp. 268-273 (reference 2) describes the latest advances that have been made in the industry to develop a process for producing flip chips using stud bumping technology. In this reference, gold bumps are formed on the I/O pads at the periphery of the IC chip by wire bonding method, and then the bumps are pressed against the
25 corresponding substrate pads. Typically, a conductive paste or anisotropic

adhesive is added to or soldering is performed on the interconnections to complete the mechanical and electrical connection between the gold bumps and the substrate. Solder material such as solder paste or solder is commonly used. Mechanical contact pressure may also be employed. The

5 chip is then encapsulated with an encapsulant such as thermosetting adhesive. Current state-of-the-art teaching, however, is that such wire bumping or stud bumping can only be applied to the non-active area of an IC chip, such as on the periphery, as discussed on page 58 of Reference 1.

The active surface of a chip is the area corresponding to the region of the

10 chip where the electronic elements such as transistors are fabricated. The main reason why stud bumping and wire bonding cannot be formed over the active area of the IC chip is because of the high risk of damage to the chip circuitry during the wire bonding process on the chip pads. Limiting the stud bumping to the inactive area of the chip severely limits the number of

15 I/O pads which can be connected to the chip and also limit the direct access to the active areas of the chip, resulting in performance limitation. In addition, inactive areas have to be provided on the chip for bonding to occur, resulting in a larger surface area requirement of the chip, reducing the productivity of a given wafer size.

20 Solder bumping involves reflowing solder bumps which have been placed between solder wettable terminals on the IC chip and the connection pads on the substrate to form solder joints. Because solder bumping can be performed over the active surface of the chip, high density area array may be achieved, allowing smaller chip design and the manufacturing of

25 packaging with very small footprints. Due to the advantages of area array

chip designs, a great need is felt in the industry to search for more ways to produce flip chip packages and area array flip chips with maximized active areas.

OBJECT OF THE INVENTION

It is an object of the present invention to provide an area array flip chip device produced by stud bumping technology where the stud bump interconnections are over the active areas of the flip chip.

- 5 It is another object of the present invention to provide a process for stud bumping connection to the on the active surface of an IC chip.

SUMMARY OF THE INVENTION

The present invention provides a flip chip device which is produced using wire bonding technology whereby the stud bump interconnections can be
10 made over the active area of the flip chip. The design and process for producing such a flip chip involves stud bumps which are bonded on the substrate, to give good electrical interconnections between the chip pads and the substrate pads. This completely eliminates the prior art limitation of not being able to have stud bump interconnections over the active area of
15 the chip, and allows the stud bump interconnection method to be applied over the entire chip area. The invention can also be applied to the joining of an IC device or first level package to a second level substrate. In this application, the stud bump process acts as a replacement for the BGA process or the solder column grid array process. In another aspect of the
20 present invention, the flip chip device produced using the stud bump interconnection according to the present invention may be electrically interconnected to a second level substrate to provide a stud bump flip chip package.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram showing a generic flip chip device.

Figures 2A to 2D are schematic diagrams to show different types of IC chip to substrate interconnections according to the present invention.

- 5 Figure 3A is a schematic diagram showing the process of chip encapsulation using a non-flow underfill encapsulant.

Figure 3B is a schematic diagram showing an example of an area array of pads over the active side of the chip without limitation.

- 10 Figure 4A shows a second level IC package of a generic wire-bonded device interconnected by stud bumping to a second level substrate according to the present invention.

Figure 4B shows a second level IC package of a generic flip chip device interconnected by stud bumping to a second level substrate according to the present invention.

- 15 Figures 5A to 5D are enlarged views showing stud bump interconnections between chip carrier and card in accordance with the present invention.

DESCRIPTION OF THE INVENTION

The present invention is a flip chip device produced by stud-bumping method, where the stud bumps are bonded to the substrate. This completely eliminates the limitation of not being able to have interconnections over the active area of the chip, and allows the stud bump interconnection method to be applied over the entire chip area to give an area array. This unexpected outcome allows wire bonding technology to be applied to area array flip chips, comparable to the flip chip solder joint interconnection method.

Figure 1 shows a diagram of a generic flip chip on a first level electronic substrate, with a semiconductor chip **20** having the active surface **22** facing downwards towards the electronic substrate **24**. Surface **25** is the exterior surface of the substrate which may also contain exterior I/O pads for interconnection with second level substrates. These first and second level substrates may be a single or multilayer organic substrate, a ceramic substrate, a printed circuit laminate in chip on board configuration, or flexible circuit substrate, including Multi-chip Module (MCM), Chip Size Package (CSP) and Ball Grid Array (BGA) modules. These substrates have a non-conducting base containing single or multilayer electrically conducting traces for electrical connection. In between the electronic substrate and the chip is the underfilling encapsulant material **26** filling the space in between the chip and the substrate. Multiple chip-to-substrate interconnections **27** between the chip pads and the substrate pads are shown.

Figures 2A to 2D shows four embodiments of the present invention, with the stud bumps 28 on the substrate pads 30 of the substrate 31 electrically connected to the corresponding chip pad 32 of the IC chip 34. Proper contact is produced using solder 36 (Figure 2A), electrically conductive paste 38 (Fig. 2B), isotropically or anisotropically conductive adhesive or anisotropically conductive film 40 (Fig. 2C). Mechanical contact 42 may also be used (Figure 2D). Encapsulant 43 is typically used to seal the joints formed using solder 36, conductive paste 38 or mechanical contact 42.

The process of producing the interconnections shown in Figure 2A involves the use of a wire bonder to form a ball at the tip of a wire, and have the ball bonded to the substrate pad using thermosonic, ultrasonic or thermo-compression bonding techniques, which are commonly used bonding techniques used to join a wire onto a chip terminal pad. The wire is then fractured just above the ball to obtain a stud bump formed over the substrate pad. If a flat bump surface is desired, coining may be performed. Multiple bumping (one bump over another) may also be performed at this stage if significant stand-off is desirable for improved resistance to stress induced and fatigue failure. On the chip side, the I/O pads are covered with a suitable interface metallurgy consisting of a single layer or multiple layer of electrically conducting films to facilitate electrical connection. Conductive pastes are then printed or injected using a dispenser onto the chip terminal pads. Conductive paste is a general term used here to mean any paste, film or adhesives which facilitates the electrical connection between the stud bump and the chip. Examples of conductive pastes are solder paste, electrically conductive paste, isotropically conductive adhesive,

anisotropically conductive adhesive and anisotropically conductive film. Alternatively, solder material may be used to facilitate the electrical connection. The chips and substrates are then appropriately aligned, assembled and joined through the application of heat as required, e.g. by solder reflow. The chip 34 and the joints could then be encapsulated with molding compounds and/or underfill materials using a liquid underfill encapsulant using capillary action as the filling process. Alternatively, a non-flow underfill encapsulant 35 as shown in Figure 3A can be used, whereby the non-flow encapsulant is applied to the substrate or chip surface before assembly and joining are performed. Using the methods described above, a group of pads or an area array of pads 44 over the active side of a chip 46 may be obtained without limitation, as shown in Figure 3B.

The process described above is also applicable to joining a device or first level package to a second level substrate to give the second level package as shown in Figure 4. In this embodiment, the stud bump process according to the present invention acts as a replacement for the BGA process in the second level packaging. Figure 4A shows schematically a chip 48 wire-bonded with wires 50 to the carrier substrate and enclosed in encapsulant 52 in the conventional way to form an IC device. In accordance with the present invention, this device may be further interconnected to a second level substrate such as a card or board 53 via stud bump interconnections 54. Figure 4B shows a generic flip chip with the chip 56 and substrate 58 interconnected via solder joints 60 and enclosed in encapsulant 62 in a conventional way. As in the case of the package shown

in Figure 4A, this package may also be further interconnected to a card or board 63 via stud bump interconnections 64.

Figures 5A to 5D show enlarged views of four embodiments of the second level stud bump interconnections. In Figures 5A and 5B, the stud bumps 65 are bonded to the I/O pad 67 of the card or board 66. Solder or
5 conductive paste 68, or anisotropic conductive adhesive or film 70 is used to complete the interconnection with the I/O pad 69 of the chip carrier or module 72. Figures 5C and 5D shows two embodiments wherein the stud bump 74 is bonded to the I/O pad 75 of the chip carrier 76. Solder or
10 conductive paste 78, or anisotropic conductive adhesive or film 80 is used to complete the interconnection with the I/O pad 81 of the card or board.

While the present invention has been described particularly with references to Figs 1 to 5, it should be understood that the figures are for illustration only and should not be taken as limitation on the invention. The
15 flip chip device provided in the present invention may be mounted on a second level substrate using methods such as ball grid array. This results in an IC package having a flip chip with stud bump interconnections over the active surface of the chip. As with other conventional substrates, the second level substrate may be made from ceramic, organic or combination material
20 having single or multilayer electrically conducting traces.

In another embodiment, the flip chip device according to the present invention may have solder balls attached to the exterior I/O pads on the exterior surface of the first level substrate. This allows convenient soldering onto a second level substrate for processing into an IC package.

The stud bumps may be made from any electrically conducting wires, such as gold, solder, copper, nickel, indium, aluminum or alloy. The substrate I/O pads may comprise of electrically conducting materials such as gold, nickel, copper, molybdenum, tungsten, chromium, aluminum, zinc, titanium or any combination of such materials.

On the chip side, the I/O pads are to be covered with a suitable interface metallurgy consisting of a single layer or multiple layer of films comprising of materials such as gold, chromium, copper, aluminum, solder, nickel, titanium, zinc or any combination of such materials. Printing or injection using a dispenser may be performed to introduce the conductive paste or adhesives or solder paste onto the chip terminal pads. Alternatively, these pastes or adhesives may be deposited onto the corresponding substrate pads. In this case, the chip I/O pads are covered with an interface and protective metallurgy to protect the IC chip bond pad metallization from contamination or corrosion. In other variations, anisotropically conductive films or adhesives may be used to join the studded substrate I/O pads to the matching chip I/O pads that are covered with appropriate interface metallurgy. Also, the surfaces could be joined mechanically after suitably preparing the surfaces to establish electrical contacts 42 (Figure 2D). The process is applicable to chips with aluminum terminal pads, as well as copper or any other terminal pads. As an alternative, solder material may also be used on the I/O pads to facilitate the electrical interconnection.

The first level substrate according to the present invention includes chip carrier or any other platform where the chips are attached to. The process is also applicable to direct chip joining to flexible substrate or board, with the

board made from materials such as inorganic (e.g. ceramic), organic or glass epoxy. These same material can be used for the second level substrate. The stud bonding may be strengthened further by modifications of the surface to be joined by plasma treatment. The interconnections envisioned in the present invention may also be used for interconnecting chip to substrate/carrier, as well as chip to board. Besides the variations described above, it is contemplated that many changes and modifications may be made by one of ordinary skill in the art without departing from the spirit and the scope of the invention described.

10 The present invention retains all the advantages of the stud bump design and process for flip chip and BGA/CSP interconnections in terms of size, weight and low cost while avoiding the serious limitation of not able to join to the active surface of the chip. In addition, existing wire bonding tools and materials may be utilized. With the wire-bonding pad pitch progressing to 50
15 microns, the present invention will allow chips and modules to achieve thousands of I/O interconnections, comparable to conventional solder joint flip chip and BGA interconnections using existing wire-bonding tools and materials.

**CLAIMS**

- 1 1. A flip chip device comprising:
 - 2 an electronic substrate having opposing first and second
 - 3 surfaces, the first surface with at least one substrate I/O pad;
 - 4 an IC chip with an active surface, said IC chip having at least one
 - 5 chip I/O pad on said active surface facing said substrate I/O pad; and
 - 6 at least one stud bump interconnection electrically interconnecting
 - 7 said IC chip I/O pad with said substrate I/O pad.
- 1 2. A flip chip device according to claim 1 wherein the stud bump
- 2 interconnection comprises a stud bump bonded to said substrate I/O
- 3 pad.
- 1 3. A flip chip device according to claim 1 or 2 wherein the electrical
- 2 interconnection is further facilitated by a conductive material.
- 1 4. A flip chip device according to claim 3 wherein the conductive
- 2 material is solder material, electrically conductive paste, isotropically
- 3 conductive adhesive, anisotropically conductive adhesive or
- 4 anisotropically conductive film.
- 1 5. A flip chip device according to claim 1 or 2 wherein the electrical
- 2 interconnection is further facilitated by mechanical contact pressure.
- 1 6. A flip chip device according to any one of the preceding claims
- 2 wherein the stud bump is made from material containing gold, solder,
- 3 copper, nickel, indium, aluminum or alloy.



- 1 7. A flip chip device according to any one of the preceding claims
2 wherein the chip I/O pad is covered with an interface metallurgy.
- 1 8. A flip chip device according to claim 7 wherein the interface
2 metallurgy of said chip I/O pad comprises at least one layer of
3 metallic film, said metallic film made from materials containing gold,
4 chromium, aluminum, solder, copper, nickel, titanium, tungsten,
5 molybdenum, vanadium, zinc or a combination thereof.
- 1 9. A flip chip device according to any one of the preceding claims
2 wherein at least one layer of the I/O pads of said substrate is made
3 from materials containing gold, nickel, copper, molybdenum,
4 tungsten, solder, chromium, vanadium, aluminum, zinc or titanium.
- 1 10. A flip chip device according to any one of the preceding claims
2 wherein said IC device further comprises an encapsulant which fills
3 the space in between the chip and the substrate.
- 1 11. A flip chip device according to claim 10 wherein the encapsulant is a
2 liquid encapsulant or a non-flow underfill encapsulant.
- 1 12. A flip chip device according to any one of the preceding claims
2 wherein the substrate is an organic substrate, a polymer substrate, a
3 flexible substrate, a ceramic substrate or a combination thereof.
- 1 13. A flip chip device according to any one of the preceding claims
2 wherein the stud bump interconnection comprises multiple bumps.
- 1 14. A flip chip device according to any one of the preceding claims
2 wherein the I/O pads of the flip chip device has an area array design.



1 15. A flip chip device according to any one of the preceding claims
2 wherein the second surface of the substrate contains at least one
3 exterior I/O pads electrically connected to a corresponding substrate
4 I/O pad on the first surface, the exterior I/O pads further having pins or
5 solder balls attached, whereby the flip chip device is adapted for
6 second level packaging.

1 16. An IC package comprising :

2 an electronic substrate having opposing first and second
3 surfaces, the first surface with at least one substrate I/O pad, the
4 second surface with at least one exterior I/O pad;

5 an IC chip with an active surface, said IC chip having at least one
6 chip I/O pad on said active surface facing said substrate I/O pad; and

7 at least one stud bump interconnection electrically interconnecting
8 said IC chip I/O pad with said substrate I/O pad

9 said exterior I/O pad of the electronic substrate further electrically
10 connected to a corresponding I/O pad of a second level substrate via
11 electrically conducting materials.

1 17. An IC package according to claim 16 wherein the electrical
2 interconnection to the second level substrate is a solder
3 interconnection.

1 18. An IC package according to claims 16 or 17 wherein the electrical
2 interconnection to the second level substrate has a ball grid array or
3 pin grid array.



- 1 19. An IC package comprising an IC device having a chip electrically
2 interconnected to a substrate, the substrate further electrically
3 connected by at least one second level electrical interconnection to
4 an I/O pad on a second level substrate, the package characterized in
5 that the second level electrical interconnection is a stud bump
6 interconnection.
- 1 20. An IC package according to claim 19 wherein the substrate
2 comprises opposing first surface and second surface, the first surface
3 having at least one I/O pad electrically interconnecting with said chip,
4 and the second surface with at least one exterior I/O pad whereto the
5 second level stud bump electrical interconnection is connected such
6 that the IC chip is electrically connected to the second level substrate.
- 1 21. An IC package according to claim 19 or 20 wherein the second level
2 electrical interconnection is further facilitated by a conductive
3 material.
- 1 22. An IC package according to claims 21 wherein the conductive
2 material is a solder material, electrically conductive paste,
3 isotropically conductive adhesive, anisotropically conductive
4 adhesive, or anisotropically conductive film.
- 1 23. An IC package according to claim 19 or 20 wherein the second level
2 electrical interconnection is further facilitated by mechanical contact
3 pressure.
- 1 24. An IC package according to any one of claims 16-23 wherein said
2 second level substrate is an electronic card, printed circuit board,



3 organic circuit board, flexible board, flexible card, flexible film,
4 ceramic substrate, polymer substrate or a combination thereof.

1 25. An IC package according to any one of claims 19-24 wherein said
2 stud bump is made from material containing gold, indium, solder,
3 copper, nickel, aluminum or alloy.

1 26. An IC package according to any one of claims 19-25 wherein said
2 second level substrate I/O pad is made from material containing
3 gold, solder, nickel, copper, molybdenum, tungsten, chromium,
4 aluminum, zinc, titanium or a combination thereof.

1 27. An IC package according to any one of claims 19-26 wherein the
2 second level electrical interconnection has an area array design or a
3 peripheral design.

1 28. A method for producing a flip chip device, said flip chip device
2 containing a chip having an active surface with at least one I/O pad, a
3 substrate having opposing first and second surfaces, said first surface
4 having at least one substrate I/O pad corresponding to said chip I/O
5 pad, said chip I/O pad and said substrate I/O pad electrically
6 interconnected by a stud bump interconnection, said second surface
7 having at least one exterior I/O pad electrically connected to the
8 corresponding substrate I/O pad,

9 said method comprising the steps of :

10 bonding a tip of a wire to the I/O pad of the substrate;



11 fracturing the wire at a point proximate the bonded wire tip to form
12 a stud bump on the I/O pad of said substrate, said stud bump adapted
13 for interconnection with said chip;

14 applying at least one layer of interface metallurgy on the I/O pad
15 of the chip;

16 aligning the chip I/O pad with the bonded stud bump; and

17 assembling the device by joining the chip to the substrate and
18 stud bump to form an electrical interconnection.

1 29. A method for producing a flip chip device according to claim 28
2 wherein an additional step of pin or solder ball placement and
3 attachment is provided whereby pins or solder balls are attached to
4 exterior I/O pads of the IC device.

1 30. A method for producing a flip chip device according to claim 28 or 29
2 wherein an additional step of applying conductive material onto the
3 stud bump or the chip substrate I/O pad is performed before the
4 joining step.

1 31. A method for producing a flip chip device according to claim 30
2 wherein said conductive material is a solder material, electrically
3 conductive paste, isotropically conductive adhesive, anisotropically
4 conductive adhesive, or anisotropically conductive film.

1 32. A method for producing a flip chip device according to any one of
2 claims 28-31 wherein an additional step of injecting an encapsulant

7 fracturing the wire at a point proximate the bonded wire tip to form
8 a stud bump on the second level substrate I/O pad, said stud bump



9 adapted for interconnection with the I/O pad on the exterior surface of
10 the device;

11 applying an electrically conductive material onto the exterior I/O
12 pad or the stud bump;

13 aligning the bonded stud bump with the corresponding I/O pad on
14 the exterior surface of the device; and

15 joining the IC device to the second level substrate via the
16 conductive material and stud bump to form an electrical
17 interconnection,

18 whereby an IC chip within the IC device is electrically connected
19 to said second level substrate.

1 38. A method for producing an IC package, said package having an IC
2 device with at least one I/O pad provided on the exterior surface of
3 the device, the device further electrically interconnected to at least
4 one I/O pad of a second level substrate via a stud bump
5 interconnection, said method comprising the steps of :

6 bonding a tip of a wire to the I/O pad on the exterior surface of the
7 device;

8 fracturing the wire at a point proximate the bonded wire tip to form
9 a stud bump on the I/O pad on the exterior surface of the device, said
10 stud bump adapted for interconnection with the I/O pad of the second
11 level substrate;



12 applying an electrically conductive material onto the second level
13 substrate I/O pad or the stud bump;

14 aligning the bonded stud bump with the corresponding second
15 level substrate I/O pad; and

16 joining the IC device to the second level substrate via the
17 conductive material and stud bump to form an electrical
18 interconnection,

19 whereby an IC chip within the IC device is electrically connected to
20 said second level substrate.

1 39. A method for producing an IC package according to claim 37 or 38
2 wherein said conductive material is a solder material, electrically
3 conductive paste, isotropically conductive adhesive, anisotropically
4 conductive adhesive, or anisotropically conductive film.

1 40. A method for producing an IC package according to claim 37-39
2 wherein said second level substrate is a polymer substrate, flexible
3 substrate a plastic substrate, a ceramic substrate or a combination
4 thereof.

1 41. A method for producing an IC package according to any one of
2 claims 37-41 wherein said wire tip is formed into a ball before
3 bonding with the I/O pad is performed.

1 42. A method for producing an IC package according to any one of
2 claims 37-41 wherein coining of the stud bump is performed to
3 smoothen the surface of the fracture point after said fracturing step.



- 1 43. A method for producing an IC package according to any one of
2 claims 37-42 wherein an additional step of injecting an encapsulant
3 between the second level substrate and the IC device is performed
4 after the joining step.
- 1 44. A method for producing an IC package according to any one of
2 claims 43 wherein said encapsulant is a non-flow underfill
3 encapsulant or a liquid encapsulant.