

**SEMICONDUCTOR ON INSULATOR TYPE STRUCTURE,
NOTABLY FOR A FRONT SIDE TYPE IMAGER,
AND METHOD OF MANUFACTURING SUCH A STRUCTURE**

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FIELD OF THE INVENTION

The present invention relates to a semiconductor on insulator type structure, notably for a “front side” type imager, an imager incorporating such a structure, and a method of manufacturing such a structure.

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PRIOR ART

Semiconductor on insulator type structures (SeOI), which successively comprise a support substrate, an electrically insulating layer and a thin semiconductor layer, have numerous applications in the field of microelectronics, optics and optoelectronics.

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One of these applications concerns imagers.

The document US 2016/0118431 describes a “front side” type imager.

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As illustrated in figure 1, said imager comprises an SOI (Silicon-On-Insulator) type structure comprising, from its rear side to its front side, a silicon support substrate 1' having a certain doping, a silicon oxide layer 2', and a monocrystalline silicon layer 3' designated active layer having a doping which can be different from that of the support substrate 1', in which is arranged a matrix array of photodiodes each defining a pixel.

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However, such an imager has low sensitivity in the near infrared, that is to say for wavelengths comprised between 700 nm and 3 μ m.

Indeed, the active silicon layer 3' has a coefficient of absorption which decreases markedly with the wavelength of the radiation to which it is exposed, namely from around 10^6 cm^{-1} for a wavelength of 300 nm to several 10^3 cm^{-1} from 700 nm.

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However, monocrystalline silicon is at the moment the favoured material to form the active layer of the substrate for the imager, because it has the advantage of being compatible with microelectronic methods enabling the manufacture of the imager and of presenting a crystalline quality (notably an absence of dislocations) suitable to the function of the active layer.

To improve the sensitivity of the imager in the near infrared, monocrystalline silicon-germanium (SiGe) is another material that could be considered for the active layer, because it advantageously has a coefficient of absorption in the near infrared that increases with increasing germanium content thereof.

5 In so far as a bulk monocrystalline silicon-germanium substrate does not exist, the formation of a monocrystalline SiGe layer of sufficient thickness (of the order of a micrometre) for the targeted application would involve an epitaxy of SiGe on a silicon on insulator type structure (heteroepitaxy) or on a SiGe on insulator structure – noted hereafter SiGeOI – (homoepitaxy). Such an epitaxy would typically be
10 implemented at a temperature of the order of 900°C. In both cases, the support substrate of the structure would be made of silicon.

Yet, due to the stress in the silicon-germanium which is compressed when a critical thickness described later is not exceeded, the epitaxial structure undergoes a deformation that results in a bow, defined as being the distance between the centre
15 of the structure and a plane containing the edge of the structure, which can reach values well above 250 µm. Yet, a structure having such a bow would be difficult to handle with conventional industrial tools, which are designed for flat substrates.

The document EP 2 251897 is interested in the compensation of the deformation caused by epitaxy of a silicon-germanium layer on the front side of a
20 silicon substrate. To this end, this document proposes a method wherein a SiGe layer is deposited on the rear side of the silicon substrate, in such a way as to compensate the deformation brought about by the deposition of the SiGe layer on the front side of the substrate. More specifically, this method comprises the following successive steps:

- 25 (a) simultaneously polishing both faces (DSP, acronym for “double side polishing”) of the silicon substrate until a suitable thickness is obtained given the thickening caused by the later deposition of SiGe layers on the front and rear sides,
(b) forming by epitaxy a SiGe layer on the rear side of the silicon substrate, so as to cause a deformation that will be compensated by the later deposition of the
30 SiGe layer on the front side,
(c) polishing and cleaning the front side of the silicon substrate,
(d) forming by epitaxy a SiGe layer on the front side of the silicon substrate.

However, this method is applied to a bulk silicon substrate having a thickness of several hundreds of micrometres, but it is not applicable to an SOI or SiGeOI type

structure, of which the thickness of the silicon or SiGe layer is of the order of a micrometre, because the double side polishing step would destroy the thin layer.

Furthermore, at the end of step (b), the structure is highly deformed, which makes it difficult to handle with a view to the polishing and the formation by epitaxy of the SiGe layer on the front side of the silicon substrate.

There thus exists a need to enable epitaxy of monocrystalline SiGe on an SOI or SiGeOI type structure which can preserve the flatness of the structure throughout the manufacture thereof.

SUMMARY OF THE INVENTION

Embodiments of the invention seek to overcome the aforementioned problem and to propose a semiconductor on insulator type substrate comprising an epitaxial SiGe layer – or more generally a monocrystalline semiconductor layer having a state of mechanical stress – and making it possible to compensate the deformation induced by said stress. Notably, this structure may be able to be used for a front side type imager to increase the absorption of light in the near infrared while respecting the constraints of compatibility with the method of manufacturing the imager and the crystalline quality of the active layer.

An aspect of the invention provides a semiconductor on insulator type structure, notably for a front side type imager, successively comprising from its rear side to its front side a semiconductor support substrate, an electrically insulating layer and a monocrystalline semiconductor layer designated active layer, characterised in that the active layer is made of a semiconductor material having a state of mechanical stress with respect to the support substrate, and in that said support substrate comprises, on its rear side, a silicon oxide layer, the thickness of said oxide layer being chosen to compensate the bow induced by the mechanical stress between the active layer and the support substrate during cooling of the structure after the formation by epitaxy of at least a part of the active layer on the support substrate.

“Front side” is taken to mean in the present text the side of the imager intended to be exposed to light radiation, which is located on the same side of the substrate as the associated electronic components.

A “state of mechanical stress with respect to the support substrate” is taken to mean in the present text that the considered layer has a compressive or extensive stress different from that potentially present in the support substrate, and capable of

inducing a deformation of the assembly formed of said layer and the support substrate at room temperature (room temperature being defined as a temperature comprised between 20 and 25°C). This state of mechanical stress is due notably to a difference in coefficient of thermal expansion between said layer and the support substrate.

According to a preferred embodiment, the active layer is a silicon-germanium layer.

Advantageously, the germanium content of the active layer is less than or equal to 10%.

Preferably, the thickness of the active layer is less than a critical thickness defined as being a thickness beyond which relaxation of the material of the active layer takes place.

According to one embodiment, the structure further comprises a silicon layer between the electrically insulating layer and the active layer.

According to one embodiment, the electrically insulating layer is made of silicon oxide.

The thickness of said electrically insulating layer is typically comprised between 10 and 200 nm.

The thickness of the silicon oxide layer situated on the rear side of the substrate is advantageously comprised between 0.5 μm and 4 μm .

Embodiments of the invention also relate to a front side imager comprising such a structure and a matrix array of photodiodes in the active layer of said structure.

Another aspect of the invention provides a method of manufacturing such a semiconductor on insulator type structure successively comprising from its rear side to its front side a semiconductor support substrate, an electrically insulating layer, and a monocrystalline semiconductor layer called active layer. Said method comprises the following steps:

- supplying a donor substrate comprising a semiconductor material suitable for the epitaxial growth of the material of the active layer;

- supplying the support substrate;

wherein the electrically insulating layer is formed on the donor substrate or on the support substrate,

- bonding the donor substrate on the support substrate, the electrically insulating layer being at the bonding interface;

- after said bonding, thinning the donor substrate so as to transfer a layer of the semiconductor material onto the front side of the support substrate;

- after said thinning, depositing a silicon oxide layer on the rear side of the support substrate,

- after said deposition of the silicon oxide layer, epitaxially growing, on the transferred layer of semiconductor material, the active layer, at a temperature greater than the deposition temperature of the oxide layer,

wherein the silicon oxide layer has a thickness chosen to compensate a bow induced by mechanical stress between the active layer and the support layer during cooling of the structure after the epitaxial growth of the active layer on the support substrate.

According to a preferred embodiment, the active layer is made of silicon-germanium.

According to one embodiment of the invention, the semiconductor material of the donor substrate suitable for the epitaxial growth of silicon-germanium is silicon-germanium.

Said semiconductor material is formed by epitaxy on a base substrate, said semiconductor material and the base substrate together forming the donor substrate.

According to another embodiment, the semiconductor material of the donor substrate suitable for the epitaxial growth of silicon-germanium is silicon.

The thickness of the silicon layer transferred onto the support substrate is advantageously less than or equal to 400 nm.

At the end of the epitaxial growth of silicon-germanium, the silicon layer may be kept between the electrically insulating layer and the silicon-germanium layer.

Alternatively, the method may comprise a step of condensation of the silicon-germanium of the active layer so as to convert the silicon layer from which the epitaxial growth of silicon-germanium has been carried out into a silicon-germanium layer.

According to one embodiment, the method comprises a step of forming an embrittlement zone in the donor substrate so as to delimit a layer of the semiconductor material suitable for the epitaxial growth of the material of the active layer, and the thinning of the donor substrate comprises a detachment along said embrittlement zone.

The formation of said embrittlement zone advantageously comprises an implantation of atomic species in the donor substrate.

The epitaxy temperature of the active layer is generally comprised between 600 and 1100°C.

The deposition temperature of the silicon oxide layer is typically comprised between 100 and 400°C.

In a particularly advantageous manner, the thickness of the silicon oxide layer is selected such that the stress generated during cooling of the structure after the deposition of said layer due to the difference in coefficient of thermal dilatation with the support substrate causes a bow less than a limit value.

DESCRIPTION OF THE FIGURES

Other characteristics and advantages of the invention will become clear from reading the detailed description that follows, with reference to the appended drawings, in which:

- 5 - figure 1 is a sectional view of an SOI structure for front side imager as described in the document US 2016/0118431;
- figure 2 is a sectional view of a structure according to one embodiment of the invention;
- figure 3 shows the coefficient of absorption of silicon-germanium as a function of wavelength for different germanium contents;
- 10 - figure 4 shows the critical thickness of a silicon layer-germanium as a function of the germanium content thereof;
- figure 5 represents the bow of a silicon substrate with a stressed SiGe layer epitaxied on its front side; this bow is plotted as a function of the stress in the SiGe and the thickness of SiGe;
- 15 - figure 6 is a sectional view of a substrate according to an alternative embodiment of the invention;
- figures 7A to 7G illustrate the main steps of a method of manufacturing a structure according to one embodiment of the invention;
- figures 8A to 8C illustrate the steps of an alternative of the manufacturing
- 20 method illustrated in figures 7A to 7F;
- figures 9A to 9E illustrate the main steps of a method of manufacturing a structure according to another embodiment of the invention;
- figure 10 is a sectional view of a pixel of a "front side" type imager comprising a structure according to one embodiment of the invention.
- 25 For reasons of legibility of the figures, the different layers are not necessarily represented to scale.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

30 Figure 2 is a sectional view of a semiconductor on insulator substrate according to one embodiment of the invention. Such a substrate can notably be used for the manufacture of a front side type imager, but is not limited to such an application.

Said substrate successively comprises, from its rear side to its front side, a silicon oxide (SiO₂) layer 4, a semiconductor support substrate 1, an electrically

35 insulating layer 2 and a monocrystalline semiconductor layer 3, called active layer.

In the remainder of the description, it will be considered that the layer 3 is a silicon-germanium (SiGe) layer, but the invention is not limited to this material, the active layer also being able to be formed of another semiconductor material, such as germanium or a III-V material, having a state of mechanical stress with respect to the support substrate.

The support substrate 1 is generally obtained by cutting a monocrystalline ingot. Advantageously, the substrate 1 is made of silicon.

According to one embodiment, the electrically insulating layer is a silicon oxide layer.

Advantageously, the thickness of said electrically insulating layer is comprised between 10 and 200 nm.

The layer 3 is intended to form the active layer of an electronic, optic or optoelectronic component. Thus, in application to an imager, the layer 3 is intended to receive a matrix array of photodiodes (not represented) enabling the capture of images. The thickness of the layer 3 is typically greater than or equal to 1 μm . Said layer 3 may be lightly doped.

As may be seen in figure 3, which illustrates the coefficient of absorption (in cm^{-1}) of SiGe as a function of wavelength (in μm) for different compositions of said material, the coefficient of absorption, notably in the infrared, increases with the germanium content.

However, the design of the layer 3 does not only concern the concentration of germanium but also the thickness of said layer. Indeed, since the SiGe layer is formed by epitaxy on a silicon substrate, the lattice parameter of which is different from that of silicon-germanium, relaxation of the SiGe layer takes place beyond a certain thickness, designated critical thickness. This relaxation results in the formation of dislocations within the SiGe layer.

Such dislocations would make the SiGe layer inappropriate for the function of the active layer 3 and must thus be avoided.

As shown in figure 4, which illustrates the critical thickness (in $\text{\AA}$) of a SiGe layer as a function of the germanium content (stoichiometric coefficient x corresponding to the composition $\text{Si}_{1-x}\text{Ge}_x$), the critical thickness is all the smaller the greater the germanium concentration.

The thickness of the active layer 3 and the germanium concentration of said layer thus result from a compromise between:

- on the one hand, a sufficiently large thickness to capture a maximum of photons in the wavelengths of the near infrared,

- on the other hand, a sufficient concentration of germanium to increase the capacity to absorb photons by the active layer in particular in the near infrared, and

5 - a limited thickness (dependent on the concentration) to avoid silicon-germanium relaxation and the creation of crystalline defects (dislocations) that result therefrom.

Typically, it is sought to maximise the thickness and the germanium concentration of the layer 3 in order to have the best possible absorption in the
10 infrared,

Preferably, the germanium content of the active layer is less than or equal to 10%. Figure 4 shows in fact that the critical thickness of a $\text{Si}_{0.9}\text{Ge}_{0.1}$ layer is of the order of a micrometre, which is suitable for the active layer of a "front side" type imager.

15 Figure 5 illustrates the bow z (in μm) of a silicon substrate of 300 mm diameter and 775 μm thickness as a function of the thickness x (in μm) of a SiGe layer deposited by epitaxy on said substrate, and the stress y (in GPa) in the SiGe layer, said stress depending on the germanium content and the thickness of the SiGe layer.

20 Thus, for example, a SiGe layer of 5 μm thickness inducing a stress of 0.1 GPa causes a bow of the order of +300 μm .

The silicon oxide layer 4 arranged on the rear side of the support substrate 1 makes it possible to compensate the deformation induced by the stress of the active layer.

25 As will be seen below in the description of embodiments of the method of manufacturing the structure, the silicon oxide layer is deposited on the support substrate before epitaxy of the SiGe layer, at a sufficiently low temperature so as not to deform notably the structure before the epitaxy step. Thus, the structure can still be handled by conventional industrial tools throughout its method of manufacture.

30 Examples of methods of manufacturing the structure illustrated in figure 2 will now be described.

Generally speaking, the method of manufacturing the structure comprises the following steps.

35 On the one hand, a donor substrate is supplied comprising a semiconductor material suitable for the epitaxial growth of silicon-germanium. Said material may

notably be SiGe (enabling homoepitaxy) or a material different from SiGe but having a lattice parameter sufficiently close to that of SiGe to enable the epitaxial growth thereof (heteroepitaxy). In this latter case, said semiconductor material is advantageously silicon.

5 On the other hand, a receiver substrate is supplied, and the donor substrate is bonded on the receiver substrate, an electrically insulating layer being at the bonding interface.

 The donor substrate is next thinned so as to transfer a layer of the semiconductor material onto the receiver substrate.

10 This thinning may be carried out by polishing or etching of the semiconductor material so as to obtain the thickness and the surface state desired for the epitaxy of SiGe.

 However, advantageously, before the bonding step, an embrittlement zone is formed in the semiconductor material so as to delimit a superficial layer to transfer.

15 After the bonding step, the thinning consists in detaching the donor substrate along the embrittlement zone, which leads to the transfer of the superficial layer onto the receiver substrate. Typically, the thickness of the transferred layer is less than or equal to 400 nm. Potentially, a finishing treatment of the free surface of the transferred layer is carried out in order to favour the implementation of the epitaxy,
20 this treatment being able to lead to thinning of the transferred layer.

 Next, on the rear side of the receiver substrate, a silicon oxide (SiO₂) layer is deposited. Such a deposition is implemented at a relatively low temperature, substantially less than the epitaxy temperature required to make the monocrystalline SiGe layer grow. Typically, the deposition temperature of the oxide layer is of the
25 order of 300°C, more generally comprised between 100 and 400°C. Those skilled in the art know the techniques enabling such a deposition, among which may be cited PECVD (Plasma-Enhanced Chemical Vapour Deposition).

 Considering that the coefficient of thermal expansion of silicon oxide is constant as a function of temperature, the stress induced by the deposition of said
30 layer on the receiver substrate results, after returning to room temperature, in a bow of 6 µm for 1000 Å deposited at 300°C, said bow being 18 µm for 1000 Å deposited at 950°C.

 The thickness of the deposited silicon oxide layer is chosen so that the bow obtained after returning to room temperature is less than or equal to a limit value, for
35 example less than or equal to 100 µm, which makes it possible to handle and to

measure the structure with standard microelectronic equipment. This thickness of the silicon oxide layer is typically comprised between 0.5 μm and 4 μm .

Finally, on the transferred layer of semiconductor material, which serves as seed layer, the epitaxial growth of a silicon-germanium layer is implemented until the
5 desired thickness for the active layer is obtained. This epitaxy is typically carried out at a temperature of the order of 900°C, more generally comprised between 600 and 1100°C.

Since the epitaxy is carried out at a temperature close to the glass transition temperature of the silicon oxide layer situated on the rear side, said silicon oxide
10 layer creeps during the epitaxy, which reduces the stress created by said layer. On the other hand, in so far as said layer has been taken to a temperature three times greater than that of its deposition, the stress created during its post-epitaxy cooling is also around three times greater than that created during its cooling following its deposition.

15 Consequently, the deposition of the SiGe layer induces a double phenomenon:

- a positive variation of the bow, linked to the stress created by the SiGe on the front side,
- a negative variation of the bow, induced by the stress created by the silicon
20 oxide on the rear side.

On returning to room temperature, the two variations cancel each other out, making it possible to benefit from an SOI or SiGeOI structure covered by a thick non-deformed SiGe layer.

Thereafter, since the steps that the structure has to undergo with a view to the
25 manufacture of the imager or another electronic, optic or optoelectronic component are implemented at temperatures below the SiGe epitaxy temperature, the structure will always become substantially flat again on returning to room temperature.

It will be noted that, when the seed layer is not made of SiGe, for example when it is made of silicon, at the end of the SiGe epitaxy the seed layer remains
30 under the active layer 3.

This situation is illustrated in figure 6, which corresponds to one particular embodiment of the invention. The seed layer is designated by the reference 42.

The seed layer is sufficiently thin (of a thickness less than or equal to 300 nm) compared to the thickness of the active layer so as not to affect notably the
35 properties of the active SiGe layer in terms of absorption in the infrared.

However, it is possible to remove the seed layer, for example by means of a condensation method. In a manner known per se, said method comprises an oxidation of the SiGe layer, said oxidation having the effect of consuming uniquely the silicon (to form silicon oxide) and to make the germanium migrate to the face
5 opposite to the free surface of the SiGe layer. A SiO₂ layer, which can be removed by etching, is then obtained on the surface.

According to a first embodiment, illustrated in figures 7A to 7F, the starting point is a donor substrate 30 comprising a superficial SiGe layer 31.

Said SiGe layer is typically formed by epitaxy on a base substrate 32,
10 generally made of silicon. Said SiGe layer is sufficiently thin to be stressed.

In a first version of this embodiment, an embrittlement zone is formed in the SiGe layer.

In a particularly advantageous manner, as illustrated in figure 7B, said embrittlement zone 33 is formed by implantation of atomic species (typically,
15 hydrogen and/or helium) through the free surface of the SiGe layer 31. The embrittlement zone 33 thereby delimits a SiGe layer 34 at the surface of the donor substrate.

With reference to figure 7C, a receiver substrate is moreover supplied comprising a support substrate 1 and an electrically insulating layer 2.

20 With reference to figure 7D, the donor substrate is bonded on the receiver substrate, the SiGe layer 31 and the electrically insulating layer 2 being at the bonding interface.

Next, as illustrated in figure 7E, the donor substrate is detached along the embrittlement zone. Said detachment may be initiated by any technique known to
25 those skilled in the art, such as a mechanical, chemical, and/or thermal stress.

The SiGe layer 34 is thereby transferred onto the support substrate.

With reference to figure 7F, a silicon oxide layer 4 is deposited at low temperature (of the order of 300°C) on the rear side of the support substrate 1. As indicated above, the thickness of the layer 4 is chosen so as not to generate a bow
30 greater than 100 µm on returning to room temperature, and to compensate the bow generated by the later epitaxy of the SiGe layer. The thickness of the layer 4 is for example of the order of 1.4 µm.

If need be, a surface treatment of the SiGe layer is carried out to remove defects linked to the implantation and to the detachment, and to make it sufficiently
35 smooth for the epitaxy step that is going to follow (cf. figure 7H described below).

In a second version of this embodiment, an embrittlement zone 33 is formed in the donor substrate 30 situated under the SiGe layer 31 (cf. figure 8A).

In a particularly advantageous manner, said embrittlement zone 33 is formed by implantation of atomic species (typically, hydrogen and/or helium) through the
5 free surface of the layer 30. The embrittlement zone 33 thus delimits a SiGe layer and a portion 38 of the base substrate 32 at the surface of the donor substrate.

A receiver substrate comprising a support substrate 1 and an electrically insulating layer 2 (cf. figure 7C) is moreover provided.

With reference to figure 8B, the donor substrate is bonded on the receiver
10 substrate, the SiGe layer 31 and the electrically insulating layer 2 being at the bonding interface.

Next, the donor substrate is detached along the embrittlement zone 33. Said detachment may be initiated by any technique known to those skilled in the art, such as a mechanical, chemical, and/or thermal stress.

15 The SiGe layer 31 and the portion 38 of the base substrate are thereby transferred onto the support substrate (cf. figure 8C).

A treatment of the surface created is then carried out to remove the portion 38 of the superficial donor substrate until a surface of SiGe is revealed, thereby removing defects linked to the implantation and to the detachment, and making it
20 sufficiently smooth for the epitaxy step that is going to follow.

As in figure 7E, a portion 34 of the SiGe layer 31 on the support substrate 1 is thereby obtained.

With reference to figure 7F, a silicon oxide layer 4 is deposited at low temperature (of the order of 300°C) on the rear side of the support substrate 1. As
25 indicated above, the thickness of the layer 4 is chosen so as not to generate a bow greater than 100 µm during the return to room temperature, and to compensate the bow generated by the later epitaxy of the SiGe layer. The thickness of the layer 4 is for example of the order of 1.4 µm.

As illustrated in figure 7G (step common to both versions of the embodiment),
30 epitaxy is then resumed in order to make a SiGe layer 35 grow on the transferred layer 34 which fulfils the role of seed layer, up to the desired thickness for the active layer 3, which is formed of both of the two SiGe layers 34 and 35 together. During epitaxy, it is possible to dope lightly the layer 35, according to the desired electrical properties. The doping of the layer 35 is not necessarily identical to that of the seed
35 layer 34.

During this epitaxy, which is carried out at a temperature of the order of 900-950°C, the oxide of the layer 4 creeps and relaxes the stress exerted within the structure.

On the other hand, during the return to room temperature that follows epitaxy,
5 the oxide layer 4 causes a stress which compensates that imposed by the SiGe layer deposited in the front side.

The structure illustrated in figure 2 is thereby obtained, which has a zero bow or a bow that is at least sufficiently low to enable handling of the structure by conventional tools in the microelectronics industry.

10 According to a second embodiment, illustrated in figures 9A to 9D, the well-known Smart Cut™ method is used to form an SOI substrate comprising the support substrate, the electrically insulating layer, and a silicon seed layer intended for the epitaxial growth of the SiGe layer.

To this end, a donor silicon substrate 40 covered by the electrically insulating
15 layer 2 (cf. figure 9A) is supplied, then an embrittlement zone 41 delimiting a silicon layer 42 to transfer (cf. figure 9B) is formed by implantation of atomic species.

A receiver substrate, which is typically the support substrate 1 of the final substrate, is moreover provided.

With reference to figure 9C, the donor substrate 40 is bonded on the receiver
20 substrate 1, the electrically insulating layer 2 being at the bonding interface.

Next, the donor substrate is detached along the embrittlement zone. Said detachment may be initiated by any technique known to those skilled in the art, such as a mechanical, chemical and/or thermal stress.

The silicon layer 42 is thereby transferred onto the support substrate 1 (cf.
25 figure 9D).

With reference to figure 9E, a silicon oxide layer 4 is deposited at low temperature (of the order of 300°C) on the rear side of the support substrate 1. As indicated above, the thickness of the layer 4 is chosen so as not to generate a bow greater than 100 µm during the return to room temperature, and to compensate the
30 bow generated by the later epitaxy of the SiGe layer. The thickness of the layer 4 is for example of the order of 1.4 µm.

If need be, a surface treatment of the silicon layer is carried out to remove defects linked to the implantation and to the detachment, and to make it sufficiently smooth for the epitaxy step that is going to follow.

Finally, epitaxy of SiGe on the transferred silicon layer 42 which serves as seed layer is then resumed, up to the desired thickness for the active layer 3. During epitaxy, it is possible to dope lightly the layer 3, depending on the desired electrical properties.

5 The substrate illustrated in figure 6 is thereby obtained.

As mentioned above, the silicon seed layer may be kept for the formation of the imager. Alternatively, the silicon layer may be removed by means of the aforesaid condensation method.

10 Figure 10 illustrates a part of a front side type imager comprising a substrate according to one embodiment of the invention corresponding to figure 2, but not limited thereto. Only a part of the imager corresponding to a pixel is represented in this figure, said pixel being electrically insulated from the other pixels formed in the active layer 3 by insulation trenches 7.

15 A doped region 36 of type different from that of the layer 3 is formed under the surface of the front side of the active layer 3. This region 36 forms with the active layer 3 a photodiode. A region 37 formed between the region 36 and the front side of the layer 3 advantageously has a doping level greater than that of the region 36 in order to passivate the interface. A passivation layer 6 is formed on the active layer 3 and may encapsulate elements making it possible to electrically control said pixel.

20 Potentially, other layers, such as filters, may be formed on the passivation layer 6, but they are not represented in figure 10.

The structure of the imager as such and its method of manufacture are known to those skilled in the art and will thus not be described in detail herein.

25 **REFERENCES**

US 2016/0118431

EP 2 251897

CLAIMS

1. Method of manufacturing a semiconductor on insulator type structure successively comprising from its rear side to its front side a semiconductor support substrate, an electrically insulating layer, and a monocrystalline semiconductor layer called active layer, the method comprising the following steps:

- supplying a donor substrate comprising a semiconductor material suitable for the epitaxial growth of the material of the active layer;

- supplying the support substrate;

wherein the electrically insulating layer is formed on the donor substrate or on the support substrate,

- bonding the donor substrate on the support substrate, the electrically insulating layer being at the bonding interface;

- after said bonding, thinning the donor substrate so as to transfer a layer of the semiconductor material onto the front side of the support substrate;

- after said thinning, depositing a silicon oxide layer on the rear side of the support substrate,

- after said deposition of the silicon oxide layer, epitaxially growing the active layer on the transferred layer of semiconductor material, at a temperature greater than the deposition temperature of the oxide layer,

wherein the silicon oxide layer has a thickness chosen to compensate a bow induced by mechanical stress between the active layer and the support layer during cooling of the structure after the epitaxial growth of the active layer on the support substrate.

2. Method according to claim 1, wherein the active layer is made of silicon-germanium.

3. Method according to claim 2, wherein the semiconductor material of the donor substrate suitable for the epitaxial growth of silicon-germanium is silicon-germanium.

4. Method according to claim 3, wherein said semiconductor material is formed by epitaxy on a base substrate, said semiconductor material and the base substrate together forming the donor substrate.

5. Method according to claim 2, wherein the semiconductor material of the donor substrate suitable for the epitaxial growth of silicon-germanium is silicon.

6. Method according to claim 5, wherein the thickness of the silicon layer transferred onto the support substrate is less than or equal to 400 nm.

7. Method according to one of claims 5 or 6, wherein, at the end of the epitaxial growth of silicon-germanium, the silicon layer is kept between the electrically insulating layer and the silicon-germanium layer.

8. Method according to one of claims 5 or 6, further comprising a step of condensation of the silicon-germanium of the active layer so as to convert the silicon layer from which the epitaxial growth of silicon-germanium has been carried out into a silicon-germanium layer.

9. Method according to one of claims 1 to 8, comprising a step of forming an embrittlement zone in the donor substrate so as to delimit a layer of the semiconductor material suitable for the epitaxial growth of the material of the active layer, and wherein the thinning of the donor substrate comprises a detachment along said embrittlement zone.

10. Method according to claim 8, wherein the formation of the embrittlement zone comprises an implantation of atomic species in the donor substrate.

11. Method according to one of claims 1 to 10, wherein the epitaxy temperature of the active layer is comprised between 600 and 1100°C.

12. Method according to one of claims 1 to 11, wherein the deposition temperature of the silicon oxide layer is comprised between 100 and 400°C.

13. Method according to one of claims 1 to 12, wherein the thickness of the silicon oxide layer is selected such that the stress generated during cooling of the structure after the deposition of said layer due to the difference in thermal expansion coefficient with the support substrate causes a bow less than a limit value.