

Description

FIELD OF THE INVENTION

The present invention relates to fabrication of integrated circuits and more particularly to techniques associated with the fabrication of integrated circuits.

BACKGROUND OF THE INVENTION

In the fabrication of customized integrated circuits, particularly gate arrays of the double metal layer C-MOS type, base wafers are prepared using conventional mass production techniques. The upper four layers of the customized integrated circuits are left to be specifically configured to a particular application as described by EP-A-0 113 828. These layers include a contact layer having apertures through which contact is established with semiconductors disposed therebelow, a metal I layer disposed over the contact layer, an insulation layer, termed a via layer, having apertures through which contact is established with the metal I layer, and a metal II layer, which is the upper metal layer of the integrated circuit.

Normally a passivation layer, such as SiO_2 , is provided over the metal II layer for mechanical protection as well as electrical insulation of the integrated circuit.

Upon definition of a specific application for a customized integrated circuit, the following steps are carried out:

The contact layer is covered with photoresist.

A specific mask formed for a given application for contact layer configuration is used to expose the photoresist overlying the contact layer in order to expose all of the required contacts which define electrical connections with underlying semiconductor devices.

The unwanted regions of photoresist are removed.

The portions of the contact layer underlying the regions at which photoresist has been removed are etched.

The remaining photoresist is removed.

The contact layer may be pre-configured and thus the above steps may form part of the mass production phase and not part of the specific configuration for specific applications.

After configuration of the contact layer, the metal layer is deposited and the following steps are carried out:

The metal I layer is covered with photoresist.

A specific mask formed for a given application for metal I configuration is used to expose the photoresist overlying the metal I layer in order to form all of the required metal I lines which define

electrical connections with underlying semiconductor devices.

The unwanted regions of photoresist are removed.

The portions of the metal I layer underlying the regions at which photoresist has been removed are etched.

The remaining photoresist is removed.

After configuration of the metal I layer, the via layer is deposited and the following steps are carried out:

The via layer is covered with photoresist.

A specific mask formed for a given application for via configuration is used to expose the photoresist overlying the via layer in order to expose all of the required contacts which define electrical connections with the underlying metal I layer.

The unwanted regions of photoresist are removed.

The portions of the via layer underlying the regions at which photoresist has been removed are etched.

The remaining photoresist is removed.

After configuration of the via layer, the metal II layer is deposited and the following steps are carried out:

The metal II layer is covered with photoresist.

A specific mask formed for a given application for metal II configuration is used to expose the photoresist overlying the metal II layer in order to form all of the required interconnects which define electrical connections with the underlying metal I lines.

The unwanted regions of photoresist are removed.

The portions of the metal II layer underlying the regions at which photoresist has been removed are etched.

The remaining photoresist is removed.

Following configuration of the metal II layer, the passivation layer is deposited and then typically configured using a general purpose mask in order to define windows in the passivation layer for circuit pads to which leads are connected, for electrical connections to the integrated circuit.

EP-A-0 210 397 discloses a method of forming a custom designed circuit from a standardised LSI circuit. Laser cutting is used to cut conductor segments in first and second layers. However, it is necessary for a laser welding operation to be performed in order to finalise the circuit connections. This technique is, therefore, suitable for use in the formation of prototypes but not for mass production.

SUMMARY OF THE INVENTION

The present invention seeks to provide a technique for production of customized integrated circuits from finished integrated circuit blanks whereby it is possible to selectively remove portions of the metal conductor at a plurality of metal layers in the finished integrated circuit blank using a single mask.

According to the present invention, there is provided a technique for production of customized integrated circuits comprising the steps of providing an integrated circuit blank having at least first and second metal layers separated by an insulating layer and characterised in that the two metal layers are connected vertically to one another via the insulating layer at predetermined locations, said first and second metal layers including portions arranged for selectable removal to provide desired customization of said integrated circuit blank, and thereafter etching at least said first metal layer to customize said integrated circuit blank, making it a functional device by said etch-only step.

Further in accordance with a preferred embodiment of the present invention, there is provided a technique for production of customized integrated circuit blank by providing a first photoresist layer over a metal layer on a substrate and etching said metal layer through exposed locations in said first photoresist layer and providing a second photoresist layer over said etched metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

Fig. 1 is a pictorial overlay illustrating the layout of a portion of a customizable array useful in an embodiment of the present invention;

Fig. 2 is a photomicrograph of the array illustrated in Fig. 1;

Figs. 3A - 3D are illustrative sectional views representing the various stages of a technique provided in accordance with one embodiment of the present invention; and

Fig. 4 illustrates a generalized mask useful in one embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference is now made to Figs. 1 - 3D, which illustrate a technique for manufacture of a customized integrated circuit in accordance with a preferred embodiment of the present invention.

Specifically considering Figs. 1 and 2, a portion of a customizable integrated circuit blank is seen wherein strips of the metal I layer 410 and of the metal II layer 412 are generally arranged in mutually perpendicular orientation so as to define a grid. Vias interconnecting the metal I and metal II layers are indicated at reference numeral 414 and contacts for the connection of external leads are indicated at reference numeral 416.

The metal I and metal II layers 410 and 412 are separated by insulative material, not shown, which prevents electrical contact therebetween, except at vias 414.

The arrangement of the various layers may be additionally appreciated from a consideration of Fig. 3A, which illustrates in section a portion of an integrated circuit blank. The blank includes a substrate 420 onto which is formed semiconductor material layers 422, 424, 426 and 428. A contact layer 430 is formed thereover.

A metal I layer 410 is formed over the contact layer and defines a contact 432 in electrical contact with semiconductor material 424. A via layer 434 is shown disposed over metal I layer 410, and metal II layer 412 is shown disposed over via layer 434 and extending therethrough at vias 414 into electrical contact with the metal I layer 410. A passivation layer 436 is formed over the metal II layer 412 and the via layer 434, where exposed.

It is a particular feature of the present invention that the various layers are configured such that the metal I and metal II layers are always exposed for etching at locations where removal thereof may be desired. This is seen from a consideration of Fig. 1, which shows a multiplicity of potential removal regions 438 wherein those potential removal regions for the metal I layer are not covered with the metal II layer.

The technique of the present invention will now be described with particular reference to Figs. 3A - 3D. The configuration illustrated in Fig. 3A and described hereinabove is characteristic of a integrated circuit blank which is ready for single mask specific configuration in accordance with a preferred embodiment of the invention.

In accordance with the present invention, as illustrated in Fig. 3B, a photoresist layer 440 is deposited over the passivation layer 436. Then, in accordance with a preferred embodiment of the present invention, an application-specific mask may be used to expose the photoresist layer 440 to define openings 442 in the photoresist layer. This application-specific mask defines openings 442 at desired regions selected from the potential removal regions 438 which are called for by the given application.

Following exposure of the photoresist layer, the photoresist overlying the selected removal regions

438 is removed, thereby defining the openings 442. The passivation layer 436 and the via layer 434, where present, are removed, as by etching at the regions defined by openings 442. The result of such removal is illustrated in Fig. 3C.

The metal layers, which typically include both metal I and metal II layers, are then removed at the regions underlying openings 442, as by etching. The result of this removal is illustrated in Fig. 3D and provides an application specific integrated circuit in accordance with the present invention.

If desired, an additional passivation layer may be added over the integrated circuit.

According to an alternative embodiment of the present invention, a generalized mask, such as that illustrated in Fig. 4, may initially be used to expose photoresist layer 440 at all of the potential removal regions 438. Thereafter the photoresist at the exposed region is removed and the passivation layer 436 and the via layer 434, where present, are etched at all of the exposed potential removal regions 438. The etched wafers are then covered once again with photoresist. Only thereafter is a single application-specific mask used to define those potential removal regions 438 at which metal I and/or metal II is to be removed.

One advantage of this alternative technique, particularly when a precisely formed general mask of the type illustrated in Fig. 4 is employed, is that the subsequently used single mask need not be as precise in its pattern definitions of the region to be removed, since the configuration of all of the potential removal regions has already been precisely defined by the general mask. As a further alternative, the general mask may in fact be comprised of a plurality of general masks, each specifically configured for a given metal layer, which masks are sequentially exposed.

It is a particular feature of the present invention that openings 442 define windows which relate to a particular predetermined customized configuration of a mass-produced, relatively general purpose integrated circuit blank. It is also a particular feature of the present invention that a plurality of metal layers are etched simultaneously.

In accordance with a preferred embodiment of the present invention the mask may be produced by laser radiation of chrome or any other suitable material. According to one embodiment of the invention, the application-specific single mask may be generated from the general mask by blocking the regions corresponding to non-selected potential removal regions 438.

Claims

1. A technique of production of customized integrated circuits comprising the steps of pro-

viding an integrated circuit blank having at least first and second metal layers separated by an insulating layer and characterised in that the two metal layers are connected vertically to one another via the insulating layer at predetermined locations, said first and second metal layers (410, 412) including portions arranged for selectable removal to provide desired customization of said integrated circuit blank, and thereafter etching at least said first metal layer to customize said integrated circuit blank, making it a functional device by said etch-only step.

2. A technique according to claim 1 and wherein said etching step comprises simultaneous etching of all desired locations on at least said first metal layer (410, 412).

3. A technique according to claim 1 or claim 2 and wherein said etching step comprises the step of simultaneously etching said first and second metal layers (410, 412) to customize said integrated circuit blank.

4. A technique according to claim 1 further comprising the steps of:

etching said at least first metal layer a first time to define a pattern of conductors including portions arranged for selectable removal; and thereafter

etching said at least first metal layer a second time to customize said integrated circuit blank by selectable removal of said at least first metal layer at selected ones of said portions.

5. A technique according to claim 4 and also comprising the step of depositing a non-metallic layer (436) over said at least first metal layer prior to etching said at least first metal layer a second time.

6. A technique according to claim 4 or claim 5, wherein said step of etching said at least first metal layer (410, 412) a second time comprises simultaneous etching of all desired locations on each of said at least first metal layer (410, 412).

7. A technique according to any of claims 1 - 6 and wherein said step of providing includes the step of forming an etch resistant layer (440) over said integrated circuit blank using a mask which defines etchable windows (442) over all portions of said first metal layer sought to be removed in a predetermined customization configuration.



438 is removed, thereby defining the openings 442. The passivation layer 436 and the via layer 434, where present, are removed, as by etching at the regions defined by openings 442. The result of such removal is illustrated in Fig. 3C.

The metal layers, which typically include both metal I and metal II layers, are then removed at the regions underlying openings 442, as by etching. The result of this removal is illustrated in Fig. 3D and provides an application specific integrated circuit in accordance with the present invention.

If desired, an additional passivation layer may be added over the integrated circuit.

According to an alternative embodiment of the present invention, a generalized mask, such as that illustrated in Fig. 4, may initially be used to expose photoresist layer 440 at all of the potential removal regions 438. Thereafter the photoresist at the exposed region is removed and the passivation layer 436 and the via layer 434, where present, are etched at all of the exposed potential removal regions 438. The etched wafers are then covered once again with photoresist. Only thereafter is a single application-specific mask used to define those potential removal regions 438 at which metal I and/or metal II is to be removed.

One advantage of this alternative technique, particularly when a precisely formed general mask of the type illustrated in Fig. 4 is employed, is that the subsequently used single mask need not be as precise in its pattern definitions of the region to be removed, since the configuration of all of the potential removal regions has already been precisely defined by the general mask. As a further alternative, the general mask may in fact be comprised of a plurality of general masks, each specifically configured for a given metal layer, which masks are sequentially exposed.

It is a particular feature of the present invention that openings 442 define windows which relate to a particular predetermined customized configuration of a mass-produced, relatively general purpose integrated circuit blank. It is also a particular feature of the present invention that a plurality of metal layers are etched simultaneously.

In accordance with a preferred embodiment of the present invention the mask may be produced by laser radiation of chrome or any other suitable material. According to one embodiment of the invention, the application-specific single mask may be generated from the general mask by blocking the regions corresponding to non-selected potential removal regions 438.

Claims

1. A technique of production of customized integrated circuits comprising the steps of pro-

viding an integrated circuit blank having at least first and second metal layers separated by an insulating layer and characterised in that the two metal layers are connected vertically to one another via the insulating layer at predetermined locations, said first and second metal layers (410, 412) including portions arranged for selectable removal to provide desired customization of said integrated circuit blank, and thereafter etching at least said first metal layer to customize said integrated circuit blank, making it a functional device by said etch-only step.

2. A technique according to claim 1 and wherein said etching step comprises simultaneous etching of all desired locations on at least said first metal layer (410, 412).

3. A technique according to claim 1 or claim 2 and wherein said etching step comprises the step of simultaneously etching said first and second metal layers (410, 412) to customize said integrated circuit blank.

4. A technique according to claim 1 further comprising the steps of:

etching said at least first metal layer a first time to define a pattern of conductors including portions arranged for selectable removal; and thereafter

etching said at least first metal layer a second time to customize said integrated circuit blank by selectable removal of said at least first metal layer at selected ones of said portions.

5. A technique according to claim 4 and also comprising the step of depositing a non-metallic layer (436) over said at least first metal layer prior to etching said at least first metal layer a second time.

6. A technique according to claim 4 or claim 5, wherein said step of etching said at least first metal layer (410, 412) a second time comprises simultaneous etching of all desired locations on each of said at least first metal layer (410, 412).

7. A technique according to any of claims 1 - 6 and wherein said step of providing includes the step of forming an etch resistant layer (440) over said integrated circuit blank using a mask which defines etchable windows (442) over all portions of said first metal layer sought to be removed in a predetermined customization configuration.



8. A technique according to any of claims 1 - 6 and also comprising the step of forming an etch resistant layer (440) over said integrated circuit blank using an etchable window mask which defines etchable windows (442) over all portions of at least one of said first and second metal layers (410, 412) sought to be removed in a predetermined customization configuration, prior to etching.
9. A technique according to any of claims 1 - 6 and also comprising the step of forming an etch resistant layer (440) over said integrated circuit blank using an etchable window mask to define etchable windows (442) over portions of at least one of said first and second metal layers which could be removed in a predetermined customization configuration, prior to etching.
10. A technique according to any of claims 7, 8 and 9 and wherein said step of forming an etch resistant layer (440) comprises the step of forming an insulating layer over said first metal layer.
11. A technique according to any of claims 7, 8, 9 and 10 and wherein said step of forming an etch resistant layer (440) also comprises the step of forming a photoresist layer over at least one of said first or said second metal layers.
12. A technique according to claim 2 or claim 3 and wherein said simultaneous etching step comprises the step of etching said at least first and second metal layers (410, 412) a second time to customize said integrated circuit blank by selectable removal of said at least first and second metal layers (410, 412) at selected ones of said portions arranged for selectable removal.
13. A technique according to any of the preceding claims and wherein said etching step for customizing said integrated circuit blank comprises the step of generating at least one customizing mask.
14. A technique according to claim 13 and wherein said step of generating at least one customizing mask comprises the step of laser irradiation of a mask material.
15. A technique according to claim 9 and wherein said etching step for customizing said integrated circuit blank comprises the step of generating at least one customizing mask and wherein said step of generating at least one

customizing mask comprises the step of laser irradiation of said etchable window mask.

16. A technique according to any of claims 7 - 11 and wherein said etch resistant layer (440) comprises photoresist.
17. A technique according to claim 9 and wherein said etching step for customizing said integrated circuit blank comprises the step of generating at least one customizing mask and wherein said step of generating at least one customizing mask comprises the step of ion beam irradiation of said etchable window mask.
18. A technique according to any of claims 1 - 3, and 7 to 12, and also including, prior to etching, the step of providing a photoresist layer which contacts locations on both said first and second metal layers.

Patentansprüche

1. Verfahren zum Herstellen kundenspezifischer integrierter Schaltungen, enthaltend die Schritte des Erzeugens eines Rohlings einer integrierten Schaltung und wenigstens einer ersten und einer zweiten Metallschicht, die durch eine Isolierschicht voneinander getrennt sind, dadurch gekennzeichnet, daß die zwei Metallschichten in vertikaler Richtung an vorbestimmten Stellen durch die Isolierschicht hindurch miteinander verbunden sind, wobei die erste und die zweite Metallschicht (410, 412) Abschnitte enthalten, die so angeordnet sind, daß sie selektiv entfernbar sind, damit eine gewünschte Kundenspezifizierung des Rohlings der integrierten Schaltung erhalten wird, und daß daraufhin wenigstens an der ersten Metallschicht geätzt wird, damit der Rohling der integrierten Schaltung kundenspezifisch ausgestaltet und nur durch den Ätzschritt zu einem funktionsfähigen Bauelement gemacht wird.
2. Verfahren nach Anspruch 1, bei welchem der Ätzschritt das gleichzeitige Ätzen aller gewünschten Stellen wenigstens an der ersten Metallschicht (410, 412) umfaßt.
3. Verfahren nach Anspruch 1 oder Anspruch 2, bei welchem der Ätzschritt den Schritt des gleichzeitigen Ätzens der ersten und der zweiten Metallschicht (410, 412) zur kundenspezifischen Ausgestaltung des Rohlings der integrierten Schaltung umfaßt.



4. Verfahren nach Anspruch 1, ferner enthaltend die Schritte:
 Ätzen wenigstens der ersten Metallschicht ein erstes Mal, um ein Muster aus Leitern einschließlich von Abschnitten zum auswählbaren Entfernen zu definieren; und danach Ätzen wenigstens der ersten Metallschicht ein zweites Mal, um den Rohling der integrierten Schaltung kundenspezifisch auszugestalten, indem wenigstens die erste Metallschicht an ausgewählten Abschnitten in auswählbarer Weise entfernt wird.

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5. Verfahren nach Anspruch 4, ferner enthaltend den Schritt des Aufbringens einer nichtmetallischen Schicht (436) wenigstens über der ersten Metallschicht vor dem zweimaligen Ätzen der wenigstens ersten Metallschicht.

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6. Verfahren nach Anspruch 4 oder Anspruch 5, bei welchem der Schritt des Ätzens der wenigstens ersten Metallschicht (410, 412) ein zweites Mal das gleichzeitige Ätzen aller gewünschten Stellen auf jeder der wenigstens ersten Metallschicht (410, 412) umfaßt.

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7. Verfahren nach einem der Ansprüche 1 bis 6, bei welchem der Schritt des Herstellens den Schritt des Bildens einer ätzbeständigen Schicht (440) über dem Rohling der integrierten Schaltung unter Verwendung einer Maske enthält, die ätzbare Fenster (442) über allen Abschnitten der ersten Metallschicht definiert, die in einer vorbestimmten Konfiguration zur kundenspezifischen Ausgestaltung entfernt werden sollen.

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8. Verfahren nach einem der Ansprüche 1 bis 6, ferner enthaltend den Schritt des Erzeugens einer ätzbeständigen Schicht (440) über dem Rohling der integrierten Schaltung unter Verwendung einer ätzbaren Fenstermaske, die ätzbare Fenster (442) über allen Abschnitten wenigstens einer der ersten und zweiten Metallschichten (410, 412) definiert, die vor dem Ätzen in einer vorbestimmten Konfiguration zur kundenspezifischen Ausgestaltung entfernt werden sollen.

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9. Verfahren nach einem der Ansprüche 1 bis 6, ferner umfassend den Schritt des Erzeugens einer ätzbeständigen Schicht (440) über dem Rohling der integrierten Schaltung unter Verwendung einer ätzbaren Fenstermaske zum Definieren ätzbarer Fenster (442) über Abschnitten wenigstens einer der ersten und zweiten Metallschichten, die vor dem Ätzen in einer vorbestimmten Konfiguration zur kundenspezifischen Ausgestaltung entfernt werden könnten.

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10. Verfahren nach einem der Ansprüche 7, 8 und 9, bei welchem der Schritt des Erzeugens einer ätzbeständigen Schicht (440) den Schritt des Erzeugens einer Isolierschicht über der ersten Metallschicht umfaßt.

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11. Verfahren nach einem der Ansprüche 7, 8, 9 und 10, bei welchem der Schritt des Erzeugens einer ätzbeständigen Schicht (440) auch den Schritt des Erzeugens einer Photoresistschicht über wenigstens einer der ersten oder zweiten Metallschichten umfaßt.

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12. Verfahren nach Anspruch 2 oder Anspruch 3, bei welchem der gleichzeitige Ätzschritt den Schritt des Ätzens der wenigstens ersten und zweiten Metallschichten (410, 412) ein zweites Mal umfaßt, um den Rohling der integrierten Schaltung kundenspezifisch auszugestalten, indem in auswählbarer Weise die wenigstens ersten und zweiten Metallschichten (110, 112) an ausgewählten Abschnitten entfernt werden, die zum auswählbaren Entfernen angeordnet sind.

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13. Verfahren nach einem der vorhergehenden Ansprüche, bei welchem der Ätzschritt zur kundenspezifischen Ausgestaltung den Schritt des Erzeugens einer Maske zur kundenspezifischen Ausgestaltung umfaßt.

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14. Verfahren nach Anspruch 13, bei welchem der Schritt des Erzeugens wenigstens einer Maske zur kundenspezifischen Ausgestaltung den Schritt der Laserbestrahlung eines Maskenmaterials umfaßt.

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15. Verfahren nach Anspruch 9, bei welchem der Ätzschritt zur kundenspezifischen Ausgestaltung des Rohlings der integrierten Schaltung den Schritt des Erzeugens wenigstens einer Maske zur kundenspezifischen Ausgestaltung umfaßt und bei welchem der Schritt des Erzeugens wenigstens einer Maske zur kundenspezifischen Ausgestaltung den Schritt der Laserbestrahlung der ätzbaren Fenstermaske umfaßt.

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16. Verfahren nach einem der Ansprüche 7 bis 11, bei welchem die ätzbeständige Schicht (440) ein Photoresist ist.

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17. Verfahren nach Anspruch 9, bei welchem der Ätzschritt zur kundenspezifischen Ausgestaltung des Rohlings der integrierten Schaltung

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den Schritt des Erzeugens wenigstens einer Maske zur kundenspezifischen Ausgestaltung umfaßt und bei welchem der Schritt des Erzeugens wenigstens einer Maske zur kundenspezifischen Ausgestaltung den Schritt der Ionenstrahlbestrahlung der ätzbaren Fenstermaske umfaßt.

18. Verfahren nach einem der Ansprüche 1 bis 3 und 7 bis 12, ferner enthaltend vor dem Ätzen den Schritt des Erzeugens einer Photoresistschicht, die Stellen sowohl auf der ersten als auch auf der zweiten Metallschicht berührt.

Revendications

1. Technique de fabrication de circuits intégrés personnalisés comprenant les étapes de préparation d'une ébauche de circuit intégré ayant au moins une première et une deuxième couches métalliques séparées par une couche isolante et caractérisée en ce que les deux couches métalliques sont connectées verticalement l'une à l'autre à travers la couche isolante à des emplacements prédéterminés, lesdites première et deuxième couches métalliques (410, 412) comprenant des parties disposées pour permettre l'élimination au choix afin de réaliser la personnalisation souhaitée de ladite ébauche de circuit intégré et de graver au moins ladite première couche métallique pour personnaliser ladite ébauche de circuit intégré en la transformant en un dispositif fonctionnel par ladite étape unique de gravure.
2. Technique selon la revendication 1 dans laquelle ladite étape de gravure comprend la gravure simultanée de tous les emplacements souhaités sur au moins ladite première couche métallique (410, 412).
3. Technique selon la revendication 1 ou la revendication 2 dans laquelle ladite étape de gravure comprend l'étape de gravure simultanée desdites première et deuxième couches métalliques (410, 412) afin de personnaliser ladite ébauche de circuit intégré.
4. Technique selon la revendication 1 comprenant en outre les étapes suivantes:
graver au moins ladite première couche métallique une première fois pour définir un motif de conducteurs englobant des parties disposées pour permettre une élimination au choix et ensuite
graver au moins ladite première couche métallique une deuxième fois pour personnaliser ladite ébauche de circuit intégré par élimination au choix d'au moins ladite première couche métallique à des endroits choisis desdites parties.
5. Technique selon la revendication 4 comprenant également l'étape consistant à déposer une couche non-métallique (436) sur au moins ladite première couche métallique avant de graver au moins ladite première couche métallique une deuxième fois.
6. Technique selon la revendication 4 ou la revendication 5 dans laquelle ladite étape consistant à graver au moins ladite première couche métallique (410, 412) une deuxième fois comprend la gravure simultanée de tous les emplacements souhaités sur chacune d'au moins ladite première couche métallique (410, 412).
7. Technique selon l'une quelconque des revendications 1 à 6 dans laquelle ladite étape de préparation comprend l'étape consistant à former une couche résistante à la gravure (440) par-dessus ladite ébauche de circuit intégré en utilisant un masque définissant des fenêtres gravables (442) par-dessus toutes les parties de ladite première couche métallique qui doivent être enlevées suivant une configuration personnalisée prédéterminée.
8. Technique selon l'une quelconque des revendications 1 à 6 et comprenant entre autres l'étape de former une couche résistante à la gravure (440) par-dessus ladite ébauche de circuit intégré en utilisant un masque de fenêtre gravable définissant des fenêtres gravables (442) par-dessus toutes les parties d'au moins l'une desdites première et deuxième couches métalliques (410, 412) qui doivent être enlevées suivant une configuration personnalisée prédéterminée, avant la gravure.
9. Technique selon l'une quelconque des revendications 1 à 6 comprenant en outre l'étape de former une couche résistante à la gravure (440) par-dessus ladite ébauche de circuit intégré en utilisant un masque de fenêtre gravable afin de définir les fenêtres gravables (442) par-dessus des parties d'au moins l'une desdites première et deuxième couches métalliques qui peuvent être enlevées suivant une configuration personnalisée prédéterminée, avant la gravure.
10. Technique selon l'une quelconque des revendications 7, 8 et 9 dans laquelle ladite étape de formation d'une couche résistante à la gravure (440) comprend l'étape de former une couche isolante par-dessus ladite première couche



métallique.

11. Technique selon l'une quelconque des revendications 7, 8, 9 et 10 dans laquelle ladite étape de formation d'une couche résistant à la gravure (440) comprend également l'étape de former une couche photorésistante par-dessus au moins l'une desdites première ou deuxième couche métallique. 5
12. Technique selon la revendication 2 ou la revendication 3 dans laquelle ladite étape de gravure simultanée comprend l'étape consistant à graver au moins lesdites première et deuxième couches métalliques (410, 412) une deuxième fois afin de personnaliser ladite ébauche de circuit intégré par élimination au choix desdites première et deuxième couches métalliques au moins (410, 412) dans des parties choisies desdites parties disposées pour leur élimination au choix. 10 15 20
13. Technique selon l'une quelconque des revendications précédentes dans laquelle ladite étape de gravure pour personnaliser ladite ébauche de circuit intégré comprend l'étape consistant à préparer au moins un masque de personnalisation. 25
14. Technique selon la revendication 13 dans laquelle ladite étape de préparer au moins un masque de personnalisation comprend l'étape de traiter un matériau de masque par rayonnement laser. 30 35
15. Technique selon la revendication 9 dans laquelle ladite étape de gravure pour personnaliser ladite ébauche de circuit intégré comprend l'étape de préparer au moins un masque de personnalisation et dans laquelle ladite étape de produire au moins un masque de personnalisation comprend l'étape consistant à traiter par rayonnement laser ledit masque à fenêtre gravable. 40 45
16. Technique selon l'une quelconque des revendications 7 à 11 dans laquelle ladite couche résistant à la gravure (440) comprend une couche photorésistante. 50
17. Technique selon la revendication 9 dans laquelle ladite étape de gravure pour personnaliser ladite ébauche de circuit intégré comprend l'étape de préparer au moins un masque de personnalisation et dans laquelle ladite étape consistant à préparer au moins un masque de personnalisation comprend l'étape de traiter ledit masque à fenêtre gravable par rayonne- 55

ment d'un faisceau d'ions.

18. Technique selon l'une quelconque des revendications 1 à 3 et 7 à 12 et comprenant en outre, avant la gravure, l'étape de disposer une couche photorésistante qui vient en contact avec des emplacements des deux dites première et deuxième couches métalliques.