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(54) SEMICONDUCTOR DEVICES AND METHODS OF MAKING SEMICONDUCTOR DEVICES

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and further relates to methods of making semiconductor devices.

The present application is divided from our co-pending Patent Application 31839/71, (Serial No. 1364676), to which reference is invited.

According to a first aspect of the present invention there is provided a semiconductor device comprising a semiconductor substrate, an epitaxial layer formed on the substrate, a buried region at the interface of the epitaxial layer and the substrate and extending partially into the epitaxial layer, a dielectrically isolating region surrounding a portion of the epitaxial layer and extending to a depth wherein it meets the buried region but not so deep as to meet the substrate, and a semiconductor circuit component formed in the isolated portion of the epitaxial layer.

The semiconductor circuit component may be a transistor having emitter and base regions within the isolated portion of the epitaxial layer. The buried region may be long to the collector of the transistor.

According to a second aspect of the present invention there is provided a method of making semiconductor devices, comprising forming a semiconductor region within a semiconductor substrate, growing an epitaxial layer on the surface of the substrate in a manner which causes a movement of impurities from the said region into the epitaxial layer during its growth, which movement results in an extension of the region into the epitaxial layer to form a

buried region located partially within the substrate and partially within the epitaxial layer, forming a protective layer on the surface of the epitaxial layer where it is subsequently intended to form a semiconductor device, oxidizing the unprotected area of the surface of the epitaxial layer to such a depth as to meet the buried region but not so deep as to meet the substrate, removing the protective layer, and forming a semiconductor circuit component in the isolated portion of the epitaxial layer.

Embodiments of the various aspects of the present invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:—

Figures 1 to 4 are cross-sectional views of portions of a semiconductor device body at successive stages in the manufacture of a first semiconductor device in accordance with the invention, and

Figure 5 is a cross-sectional view of a portion of a semiconductor body of a second semiconductor device in accordance with the invention.

In the embodiment now to be described with reference to Figures 1 to 4, the starting material is a monocrystalline semiconductor substrate body 61 of *p*-type silicon, in which by means of conventional planar methods arsenic-doped low-ohmic *n*-type regions 62 and a boron-doped low-ohmic *p*-type region 63 are formed. The region 63 has the form of a network, and may enclose the regions 62 laterally. The parts of said region 63 may have a width of 3 μ . The resulting stage is shown in Figure 1. As is usual in planar diffusion methods, an oxide layer 64 is present on the surface of the semiconductor body 61. This oxide layer is now removed in normal manner by means of hydrofluoric acid.

A high-ohmic *n*-type epitaxial layer 68, for example 4 μ thick, is then deposited on the silicon body 61. This deposition can be

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effected in known manner by decomposition of silane or a reaction of halogen silane with hydrogen. During this deposition the regions 62 and 63, which become buried layers, can expand in the epitaxial layer 68 by diffusion. Particularly the buried layer 63 can expand more rapidly than the buried layer 62, since boron diffuses more rapidly than arsenic.

In known manner, the surface of the epitaxial layer 68 is covered with a thin silicon nitride layer 65 and then with a silicon oxide layer 66. The silicon nitride layer 65 may be deposited by, for example, heating the body 61 with the epitaxial layer 68 at a temperature of approximately 1000° C in a gas mixture of SiH₄ and NH₃. The thickness of the silicon nitride layer is approximately 0.15 micron. Below the nitride a very thin silicon oxide layer not shown may be used, for example of approximately 500 Å. A silicon oxide layer 66 having a thickness of 0.2 micron is deposited on the silicon nitride layer 65, for example from a gas mixture consisting of a carrier gas, for example argon, with SiH₄ and oxygen. In particular the silicon nitride layer 65 serves to protect underlying silicon against oxidation in a subsequent step of locally forming the sunken insulation layer of silicon oxide.

In these oxide and nitride layers 66 and 65 apertures are provided above the *p*-type buried region 63 likewise in the form of a network. For that purpose, local apertures are first provided in the oxide layer 66 in normal manner by using photoresist and a hydrofluoric acid etchant, after which the remaining parts of said oxide layer are used as a masking for the local etching away of the nitride layer 65 with orthophosphoric acid.

The width of said aperture is at least 5μ. While using the nitride oxide masking 65, 66, grooves 67 are etched in the silicon with a depth of well over 1μ. The resulting stage is shown in Figure 2.

The oxide layer 66 is then removed by means of a conventional hydrofluoric acid etchant and the assembly is then subjected to an oxidizing treatment to form a sunken dielectric layer 70 consisting of silicon oxide, the silicon nitride masking 65 protecting the underlying silicon outside the grooves 67. The oxidizing treatment may be performed in steam at a pressure of approximately 1 atmosphere and at a temperature of approximately 1000° C. The nitride 65 protects the underlying surface of the silicon from the action of the oxidizing atmosphere. In the grooves 67, however, the steam can act on the silicon forming oxide. Since the formed silicon oxide occupies well over double the volume of the original silicon which has been converted, the oxide forming at the walls of the grooves is expanding both in the

epitaxial layer 68 and in the groove itself. After a treatment time of approximately 16 hours, a sunken oxide layer 70 is formed in the grooves to a depth of 2μ, the oxide filling the original grooves 67 substantially entirely. Further details on this and other methods for sinking an oxide into a semiconductor may be found in Canadian Patent No. 826,343, U.S. Patent No. 3,544,858, and Philips Research Reports, 25, 118—132, April 1970.

During the oxidation treatment, the boron-doped *p*-type buried layer 63 has further expanded in the epitaxial layer. In that stage, or after subsequent heating treatment, it adjoins the lower side of the formed sunken insulation layer 70. The resulting stage is shown in Figure 3. The epitaxial layer 68 is now divided into island portions which are separated from each other by means of isolation regions formed by the sunken insulation layer 70 and the buried *p*-type layer 63.

In known manner, for example, by means of planar diffusion methods, semiconductor circuit components can be formed in the islands. For example, the *n-p-n* transistor shown in Figure 4 has an *n*-type collector provided by the epitaxial *n*-type material 78 and the arsenic-doped buried layer 62. A collector contact region 77 is formed during the emitter diffusion. The base is provided by a *p*-type region 75 formed by diffusion of boron. The emitter is provided by an *n*-type region 76 formed by diffusion of phosphorus. The resulting stage is shown in Figure 4.

Since it has been ensured during the manufacture that the sunken insulation layer became wider than the buried *p*-type layer 63, the distance between the buried layer 63 and the base region 75 is kept large notwithstanding the fact that the base layer 75 adjoins the sunken insulation layer 70.

As shown diagrammatically in Figure 4, the upper side of the insulation layer 70 is at approximately the same level as the adjacent surface of the epitaxial layer.

In the case described with reference to Figure 4, a thick epitaxial layer is used. However, for forming isolation regions, the use of correspondingly thick sunken insulation layer has been avoided, by providing the buried regions 63.

Contact windows may be provided in a thin insulation layer on the island surface through which windows contacts are made in known manner to circuit component regions, and supply conductors may be used which preferably extend as much as possible over the insulation layer 70.

It is obvious that other circuit components, for example other transistors, may also be provided in other islands present beside the

island in which the transistor shown in Figure 4 is present.

If desired, using a local interruption of the *p*-type buried layer 63, two islands can be connected electrically below the sunken insulation layer 70 via the epitaxial material 68 or via a local extension of the *n*-type layer 62. If desired, a local interruption of the sunken insulation layer 70 can also be used.

The above example described with reference to Figures 1 to 4 relates to a *p*-type substrate and an *n*-type epitaxial layer. In a corresponding manner, of course, an *n*-type substrate and a *p*-type epitaxial layer may be used as the starting material in which in a corresponding manner the various regions and buried layers can also be chosen to be of a correspondingly other conductivity type. In that case, for example, phosphorus may be used as a doping for the buried layers 63 of Figure 4, as an *n*-type doping material in silicon. Both boron and phosphorus have a very high solubility in silicon while the diffusion properties do not differ greatly.

In the embodiment of Figure 5 a monocrystalline substrate body is used having the same conductivity type as the epitaxial layer present thereon. The monocrystalline silicon substrate body 100 consists, for example, of *n*-type material having a resistivity of, for example, 1 ohm.cm. An epitaxial layer 104 present thereon consists of silicon of the same conductivity type and approximately the same resistivity. At the boundary of the substrate body and the epitaxial layer a number of buried regions in the form of layers 101, 102 and 103 of *p*-type silicon are present and are separated from each other by a network of narrow regions 111 of the high ohmic *n*-type material of the substrate and the epitaxial layer. The buried layers are doped, for example, with boron and have expanded from the boundary between the substrate 100 and the epitaxial layer 102 during the epitaxial deposition and oxidizing treatment.

From the upper side of the epitaxial layer a sunken insulation layer is provided, as already described above, the upper surface of which is approximately level with the upper side of the adjacent portions of the epitaxial layer. The sunken insulation layer 109 *inter alia* overlaps the *n*-type regions 111 between the buried layers 101, 102 and 103. However, the insulation layer 109 may also be provided locally as intermediate strips extending from the top to a, for example, more central part of a buried layer such as the layer 102. In this manner the epitaxial layer 104 is divided into *n*-type islands 105, 106, 107 and 108 which are separated from the *n*-type substrate 100 by two *p-n* junctions and are separated from

each other by isolation regions comprising portions of the sunken insulation layer 109. Thus, for example, the islands 105 and 106 are separated from each other by the sunken insulation layer 109, the parts of the buried layers 102 and 103 facing each other, and the intermediately located high-ohmic *n*-type region 111. The islands 106 and 107 are separated from each other by an intermediate portion of the sunken insulation layer 109 and the buried layer 102; however, as described hereinafter, the layer 102 may form a connection between the islands 106 and 107. The islands 107 and 108 are separated from each other by the sunken insulation layer 109, the end parts of the buried layers 101 and 102 facing each other and the intermediately located high-ohmic *n*-type region 111.

Semiconductor circuit components may be formed in known manner in these islands. Thus, by way of example, a *p*-type diffused region 112 is shown provided in the *n*-type island portion 107. An underlying buried layer 101, or 102 or 103 which actually is separated from the substrate body 100 of the *n*-type material by a *p-n* junction may both serve for isolation and form a functional part of a circuit component, for example the collector of a *p-n-p* transistor having a *p*-type emitter region and an *n*-type base region. When it is provided below more than one island, as is the buried layer 102, it may also serve as a connection. Such a buried layer connection 102 may be, for example, a common, possibly floating, electrode of two circuit components provided in the islands 106 and 107. In the arrangement shown in Figure 5, it is evident that the region 106 which reaches the buried layer 102 is isolated by a portion of the sunken oxide layer pattern 109 from other regions 113 and 107 which are also present over the buried layer 102 and within the epitaxial layer 104.

An island structure corresponding to Figure 5 can also be obtained by using a *p*-type substrate 100 on which *p*-type epitaxial material 104 is provided and in which *n*-type buried layers 101, 102 and 103 are formed.

It is to be noted that the Figures are meant to indicate that within the scope of the present invention a variety of embodiments are possible. The types of circuit components shown are not limitative. Different semiconductor circuit components may be provided, for example field effect transistors or components having contacts of the Schottky type.

A further embodiment of the invention will now be described as a modification of Figures 6, 7 and 8 of the accompanying drawings. These Figures 6, 7 and 8 correspond to Figures 1, 2 and 3 of the said co-

(Serial No. 1364676) and are diagrammatic cross-sectional views of a portion of a semiconductor device body at successive stages in the manufacture of a semiconductor device. As will be discussed hereinafter both the device and method as illustrated in Figures 6 to 8 be outside the scope of the present invention. Reference is invited to the Specification of the said co-pending Parent Application for specific details of the construction and manufacture of this semiconductor device, which will be described hereinafter only in outline:

A monocrystalline p -type silicon semiconductor substrate body 1 is provided on one side with an n -type silicon epitaxial layer 2 having a thickness of 2.5 microns, see Figure 6. Arsenic-doped $n+$ regions are locally provided previously on that side of the body 1 by planar methods known *per se* to form buried $n+$ layers 3 and 4. During the epitaxial deposition, the arsenic-doped $n+$ regions provided in the substrate expand in the epitaxial layer 2.

A layer 6 of silicon nitride is deposited in known manner on the epitaxial layer 2, and a silicon oxide layer 7 is deposited on the silicon nitride layer 6. At the area of a sunken insulation layer 20 to be formed in the epitaxial layer 2 apertures 11 are made in the nitride-oxide layers 6, 7. The resulting local masking is first used to etch grooves 8 in the epitaxial layer 2 to a depth of over 1 micron. The stage shown in Figure 6 is now obtained.

While using the nitride layer 6 for local masking, the semiconductor body is subjected to an oxidizing treatment as described hereinbefore to form in the grooves 8 the oxide layer pattern 20 sunk to a depth of 2 microns. The resulting stage is shown in Figure 7. During the oxidizing treatment, the buried layers 3 and 4 expand further in the epitaxial layer 2 by further arsenic diffusion.

The upper side of the sunken insulation layer 20 is now substantially at the same level as the upper side of the epitaxial layer 2. The lower side of the sunken insulation layer 20 is present at a distance of approximately 0.5 micron from the p - n junction 21 between the p -type substrate material 1 and the n -type material of the epitaxial layer 2.

On either side of the p - n junction 21 between the substrate 1 and the epitaxial layer 2, a depletion layer 21 is present, formed by the diffusion of charge carriers and the resulting contact potential when no external voltage is applied across said junction 21.

The thickness of the epitaxial layer 2 and the depth of the sunken insulation layer 20 may be chosen such that, without applying an external bias voltage, this depletion layer adjoins the lower side of the sunken insulation layer 20. However, preferably the de-

pletion layer at zero bias is expanded to reach the sunken oxide layer 20 during normal operation of the device. Thus sufficiently high voltage may be set up in the reverse direction across the said p - n junction during normal operation of the device that the depletion layer 21 so formed reaches sufficiently far in the epitaxial layer to form an isolation region consisting partly of the sunken insulation layer 20 and partly of the underlying part of the depletion layer 21. The extent of the depletion layer 21 is indicated by broken lines in Figures 7 and 8.

Thus the epitaxial layer 2 is divided into island portions 22 which are laterally separated from each other by an isolation region formed partly by the sunken insulation layer 20 and, at least during operation of the semiconductor device, partly by the underlying part of the depletion layer 21.

According to the notation used in Figures 6 to 8 to indicate the extension of the buried layers 3 and 4 in the epitaxial layer 2, the sunken oxide layer 20 is not shown as meeting the buried layers 3 and 4, so that with notation these Figures lie outside the scope of the present invention. However in a modification which is in accordance with the present invention, both the buried layer 3 and the buried layer 4 adjoin the sunken insulation layer 20. In this case it should be ensured that under the sunken oxide layer 20 a sufficiently wide zone of the depletion layer 21 remains to adjoin the insulation layer 20 and form with the layer 20 an effective isolation region for the islands 22.

In known manner semiconductor circuit components may be formed in the islands 22. Conventional diffusion methods may be employed. If desired, the nitride layer 6 already present may be used to provide a diffusion mask. However, this nitride layer may be removed and replaced by a fresh oxide layer, or combinations of parts of the old nitride masking layer 6 and a new oxide masking layer may simultaneously be used. If desired, the nitride layer 6 may also locally serve as an insulating surface coating in the manufactured device.

Figure 8 shows semiconductor circuit components provided in the islands 22 of the epitaxial layer 2, namely in a first island an n - p - n transistor 25, in a second island a MIS transistor 26, in a third island a diode 27, and in a fourth island a resistance element 28.

The transistor 25, for example, is obtained by local diffusion into the island beneath which there extends the buried layer 3. The base 31 is provided by acceptor diffusion, for example boron. By locally diffusing a donor, for example phosphorus, using known planar techniques, the emitter 32 is provided in the base region 31. The collector is provided by n -type material 30 of the epit-

axial layer 2 and the buried layer 3. A highly doped surface-adjointing contact region 33 to the collector is formed within the epitaxial layer 2 by donor diffusion, for example simultaneously with the emitter diffusion. The base region 31 adjoins over part of its periphery the sunken insulation layer 20. The collector contacting region 33 is present at some distance from the base 31, but also adjoins along part of its periphery the sunken insulation layer 20. The buried layer 3 is a highly-doped collector region which extends from beneath the base 31 to beneath the collector contacting region 33. The transistor 25 is provided at the surface in known manner with a thin insulation layer, for example of silicon oxide, having windows for a collector contact 34 on the collector contacting region 33, for a base contact 35, and for an emitter contact 36. Connections in the form of metal strips to the contacts 34, 35 and 36 may be provided in known manner across the insulation layers.

For details of the construction and formation of MIS field-effect transistors 26, the diode 27 and the resistor 28, and for other features and modifications of the device of Figure 8, reference is invited to the said co-pending Parent Application 31839/71, (Serial No. 1364676).

Many variations are possible without departing from the scope of the present invention. The sunken insulation layer may comprise extensions present in the islands, for example as a carrying layer for wiring. The sunken insulation layer may comprise widenings, for example serving as a carrier for a number of conductive strips, or at an area where external supply conductors can be connected, for example by soldering.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor substrate, an epitaxial layer formed on the substrate, a buried region at the interface of the epitaxial layer and the substrate and extending partially into the epitaxial layer, a dielectrically isolating region surrounding a portion of the epitaxial layer and extending to a depth wherein it meets the buried region but not so deep to meet the substrate, and a semiconductor circuit component formed in the isolated portion of the epitaxial layer.

2. A semiconductor device as claimed in Claim 1, wherein the semiconductor circuit component is a transistor, and the buried region is the collector of the transistor.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein a semicon-

ductor region which reaches the buried region is isolated by a portion of the dielectrically isolating region from other regions of the said circuit component which are present in the isolated portion of the epitaxial layer.

4. A semiconductor device as claimed in any of Claims 1 to 3, wherein the surface of the device is substantially planar.

5. A method of making a semiconductor device comprising forming a semiconductor region within a semiconductor substrate, growing an epitaxial layer on the surface of the substrate in a manner which causes a movement of impurities from the said region into the epitaxial layer during its growth, which movement results in an extension of the region into the epitaxial layer to form a buried region located partially within the substrate and partially within the epitaxial layer, forming a protective layer on the surface of the epitaxial layer where it is subsequently intended to form a semiconductor device, oxidizing the unprotected area of the surface of the epitaxial layer to such a depth as to meet the buried region but not so deep as to meet the substrate, removing the protective layer, and forming a semiconductor circuit component in the isolated portion of the epitaxial layer.

6. A method as claimed in Claim 5, wherein the said region is of a first conductivity type and the semiconductor substrate is of a second conductivity type.

7. A method as claimed in Claim 5 or Claim 6, wherein the unprotected areas are etched to a predetermined depth prior to the oxidizing step.

8. A method as claimed in any of Claims 5 to 7, wherein a protection layer is also formed where a further region reaching the buried region is required, and wherein after oxidation this further region is dielectrically isolated from other unoxidized semiconductor surface regions.

9. A method as claimed in any of Claims 5 to 8, wherein the semiconductor circuit component is a transistor, and the buried region serves as a collector region of the transistor.

10. A method as claimed in any of Claims 5 to 9, wherein the protective layer comprises silicon nitride and the semiconductor material is silicon.

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2. A semiconductor device as claimed in Claim 1, wherein the semiconductor circuit component is a transistor, and the buried region is the collector of the transistor.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein a semicon-

ductor region which reaches the buried region is isolated by a portion of the dielectrically isolating region from other regions of the said circuit component which are present in the isolated portion of the epitaxial layer.

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5. A method of making a semiconductor device comprising forming a semiconductor region within a semiconductor substrate, growing an epitaxial layer on the surface of the substrate in a manner which causes a movement of impurities from the said region into the epitaxial layer during its growth, which movement results in an extension of the region into the epitaxial layer to form a buried region located partially within the substrate and partially within the epitaxial layer, forming a protective layer on the surface of the epitaxial layer where it is subsequently intended to form a semiconductor device, oxidizing the unprotected area of the surface of the epitaxial layer to such a depth as to meet the buried region but not so deep as to meet the substrate, removing the protective layer, and forming a semiconductor circuit component in the isolated portion of the epitaxial layer.

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