networking manner. For example, a cascading tree network or a ring network may be used, provided that the array controller 11 and the solid state disk 22 can communicate with each other.

[0049] The solid state disk 22 includes an SSD controller 220 and a storage medium 221. The SSD controller 220 is configured to perform an operation such as a write data request or a read data request sent by the array controller 11.

[0050] The storage medium 221 generally includes some flash memory (Flash) chips. Each flash memory chip includes multiple channels, and each channel includes some blocks (block) (as shown in FIG. 2). Generally, the flash memory chip may be divided into some blocks according to a fixed size. Therefore, a block has a standard size. The standard size of the block refers to a size of data that can be stored in a block that is idle and that includes no bad page (bad page). Generally, the standard size of the block may be the Nth power of 2 (M), where N is a positive integer. An erase operation performed by the SSD is performed in blocks. For example, when the SSD needs to perform garbage collection, the SSD may first move valid data from one block to another new block, and then erase all data (including the valid data and invalid data) stored in the original block. In this embodiment of the present invention, valid data in a block refers to data that is stored in the block and that has not been modified, and this part of data is possibly to be read; invalid data in a block refers to data that is stored in the block and that has been modified, and this part of data is impossibly to be read. It may be known by a person skilled in the art that because of an erase feature of a flash memory chip, data stored in a block is not directly modified as data in a common mechanical hard drive is. When data in a block needs to be modified, the SSD controller 220 finds a new block and writes modified data into the new block, and the data in the original block becomes invalid data. The invalid data is erased when the SSD performs garbage collection.

[0051] In addition, as shown in FIG. 3, each block includes some pages (page). The SSD writes data in pages when executing a write data request. For example, the array controller 11 sends a write data request to the SSD controller 220, where the write data request carries logical block addresses (logical block Address, LBA) and data, and the LBAs are addresses that are visible and accessible to the array controller 11. After receiving the write data request, the SSD controller 220 writes the data into pages of one or more blocks according to a set policy. Addresses of the pages into which the data is written are addresses at which the data is actually stored, and are also referred to as physical addresses. The SSD includes a flash translation layer (Flash Translation Layer, FTL), configured to establish and store a correspondence between the LBAs and the physical addresses. When the array controller 11 subsequently sends a read data request to the SSD controller 220, to request to read the data, where the read data request carries the LBAs, the SSD controller 220 may read the data according to the LBAs and the correspondence between the LBAs and the physical

addresses, and send the data to the array controller 11.

[0052] When the array controller 11 reads a segment of data from a cache, and sends the segment of data to the SSD, generally, the segment of data is a segment of data with contiguous logical addresses. However, when receiving the write data request, the SSD controller 220 writes, according to the policy set by the SSD controller 220, the data into the pages (that is, the physical addresses) of the one or more blocks. It may be understood by a person skilled in the art that actually, these physical addresses are not necessarily contiguous. That is, from the perspective of the array controller 11, the segment of data with the contiguous logical addresses is actually written into physical space of the SSD in a scattered manner. The following describes how to write data by an SSD in the prior art with reference to FIG. 4.

[0053] FIG. 4 is a schematic diagram of how to write data by an SSD in the prior art. Generally, because the solid state disk 22 may concurrently write data into channels, after the array controller 11 sends data to the solid state disk 22, the SSD controller 220 generally selects one block from each channel, and concurrently writes the data into the multiple blocks. It may be understood that the solid state disk 22 may also concurrently write the data into multiple blocks in one channel. As shown in FIG. 4, after the data is written into the multiple blocks, each block provides a part of space to store a part of the data. In FIG. 4, a white part of a block represents free space of the block, and a gray part represents used space of the block after a part of the data is written into the block. Therefore, from the perspective of the array controller 11, a segment of data with contiguous logical addresses is stored in multiple blocks in a scattered manner, and data belonging to different logical address segments is written into different blocks. It may be known by a person skilled in the art that a garbage collection operation is regularly performed in the SSD, and erasing is performed in blocks during a garbage collection operation. As the segment of data with the contiguous logical addresses is stored in the multiple blocks in a scattered manner, and the data belonging to the different logical address segments is written into the different blocks, during the garbage collection, valid data needs to be moved from multiple blocks to a free block, which increases write amplification caused by the garbage collection. The write amplification means that data written into a flash memory chip is more than data that is written by a host into an SSD.

[0054] In this embodiment, as shown in FIG. 5, one block may be taken out of each channel, to form a logical block (logical block). That is, the logical block in this embodiment includes multiple blocks, and the blocks are located in different channels. It may be understood that one block may also be taken out of each of a part of the channels, to form a logical block. Likewise, the multiple blocks included in the logical block are separately located in different channels. A size of the logical block is an integer multiple of a standard size of a block, and depends on a quantity of blocks

or a logical address range of the logical block.

[0059] The following describes a hardware structure of the array controller 11. FIG. 6 is a schematic structural diagram of the array controller 11 according to an embodiment of the present invention. As shown in FIG. 6, the array controller 11 mainly includes a processor (processor) 118, a cache (cache) 120, a memory (memory) 122, a communications bus (bus for short) 126, and a communications interface (Communications Interface) 128. The processor 118, the cache 120, the memory 122, and the communications interface 128 communicate with each other by using the communications bus 126.

[0060] The communications interface 128 is configured to communicate with the host 33 or the solid state disk 22.

[0061] The processor 118 may be a central processing unit CPU or an application specific integrated circuit ASIC (Application Specific Integrated Circuit), or is configured as one or more integrated circuits that implement this embodiment of the present invention. In this embodiment of the present invention, the processor 118 may be configured to receive a write data request or a read data request from the host 33, process the write data request or the read data request, send the write data request or the read data request to the solid state disk 22, and perform another operation.

[0062] The memory 122 is configured to store a program 124. The memory 122 may include a high-speed RAM memory, and may further include a non-volatile memory (non-volatile memory), such as at least one magnetic disk memory. It may be understood that the memory 122 may be any non-transitory (non-transitory) computer-readable medium that can store program code, such as a random access memory (Random Access Memory, RAM), a magnetic disk, a hard disk, an optical disc, a solid state disk (Solid State Disk, SSD), or a non-volatile memory.

[0063] The program 124 may include program code, where the program code includes a computer operation instruction.

[0064] The cache 120 (Cache) is configured to temporarily store data received from the host 33 or data read from the solid state disk 22. The cache 120 may be any non-transitory (non-transitory) machine-readable medium that can store data, such as a RAM, a ROM, a flash memory (Flash memory), or a solid state disk (Solid State Disk, SSD), which is not limited herein. For example, when receiving a write data request sent by the host 33, the array controller 11 may store the write data request in the cache 120, and the processor 118 processes the write data request. Optionally, when receiving multiple write data requests sent by the host 33, the array controller 11 may temporarily store the multiple write data requests in the cache 120, and when a size in the cache 120 reaches a water mark (for example, a size of data stored in the cache 120 reaches a size of a logical block), read data whose size is equal to the size of the logical block from the cache 120, and send

CLAIMS

What is claimed is:

1. An array controller, wherein the array controller is located in a storage system, the storage system comprises the array controller and a solid state disk, the solid state disk comprises a flash memory chip, and the flash memory chip comprises multiple blocks, wherein

the array controller comprises a communications interface and a processor;

the communications interface is configured to communicate with the solid state disk; and

the processor is configured to: receive information about a logical block sent by the solid state disk, wherein the information about the logical block comprises a size of the logical block and indication information of the logical block, and the logical block comprises one or more blocks; and

send multiple write data requests to the solid state disk, wherein each write data request includes target data, each write data request is used to instruct the solid state disk to write the target data into the logical block indicated by the indication information of the logical block, and a sum of lengths of the target data included in the multiple write data requests is equal to the size of the logical block.

2. The array controller according to claim 1, wherein the blocks comprised in the logical block are located in different channels.

3. The array controller according to claim 1 or 2, wherein the logical block is in a to-be-written state, and wherein the logical block in the to-be-written state indicates that the logical block has been allocated by the solid state disk to store data.

4. The array controller according to any one of claims 1 to 3, wherein the indication information of the logical block comprises an identifier that is allocated by the solid state disk to the logical block, and each write data request comprises the identifier of the logical block.

5. The array controller according to any one of claims 1 to 3, wherein the indication information of the logical block comprises a logical address range that is allocated by the solid state disk to the logical block, and each write data request comprises a sub-range of the logical address range.

6. A solid state disk, comprising: a flash memory chip and a solid state disk controller, wherein

the flash memory chip comprises multiple blocks; and

the solid state disk controller is configured to: send information about a logical block to an array controller, wherein the information about the logical block comprises a size of the logical block and indication information of the logical block, and the logical block comprises one or more blocks;

receive multiple write data requests sent by the array controller, wherein each write data request includes target data, each write data request is used to instruct the solid state disk to write the target data into the logical block indicated by the indication information of the logical block, and a sum of lengths of the target data included in the multiple write data requests is equal to the size of the logical block; and

write the target data included in each write data request into the logical block indicated by the indication information.

7. The solid state disk according to claim 6, wherein the blocks comprised in the logical block are located in different channels.

8. The solid state disk according to claim 6 or 7, wherein

the solid state disk controller is further configured to determine that the logical block is in a to-be-written state, wherein the logical block in the to-be-written state indicates that the logical block has been allocated to store data; and

allocate the indication information to the logical block in the to-be-written state.

9. The solid state disk according to any one of claims 6 to 8, wherein the indication information of the logical block comprises an identifier of the logical block, and each write data request comprises the identifier of the logical block; and

the solid state disk controller is specifically configured to write, according to the identifier of the logical block, the target data in each write data request into the logical block corresponding to the identifier.

10. The solid state disk according to any one of claims 6 to 8, wherein the indication information of the logical block comprises a logical address range of the logical block, and each write data request comprises a sub-range of the logical address range; and

the solid state disk controller is specifically configured to: determine, according to the sub-range of the logical address range in each write data request and the logical address range of the logical block, the logical block corresponding to the target data in each write data request; and

write the target data in each write data request into the corresponding logical block.

11. The solid state disk according to any one of claims 8 to 10, wherein

the solid state disk controller is further configured to reclaim the indication information allocated to the logical block after the writing the target data into the logical block indicated by the indication information.

12. A method for controlling a solid state disk to write data, wherein the method is applied to a storage system, the storage system comprises an array controller and the solid state disk, the solid state disk comprises a flash memory chip, and the flash memory chip comprises multiple blocks;

and the method is performed by the array controller and comprises:

receiving information about a logical block sent by the solid state disk, wherein the information about the logical block comprises a size of the logical block and indication information of the logical block, and the logical block comprises one or more blocks; and

sending multiple write data requests to the solid state disk, wherein each write data request includes target data, each write data request is used to instruct the solid state disk to write the target data into the logical block indicated by the indication information of the logical block, and a sum of lengths of the target data included in the multiple write data requests is equal to the size of the logical block.

13. The method according to claim 12, wherein the blocks comprised in the logical block are located in different channels.

14. The method according to claim 12 or 13, wherein the logical block is in a to-be-written state, and wherein the logical block in the to-be-written state indicates that the logical block has been allocated by the solid state disk to store data.

15. The method according to any one of claims 12 to 14, wherein the indication information of the logical block comprises an identifier that is allocated by the solid state disk to the logical block, and each write data request comprises the identifier of the logical block.

16. The method according to any one of claims 12 to 14, wherein the indication information of the logical block comprises a logical address range that is allocated by the solid state disk to the logical block, and each write data request comprises a sub-range of the logical address range.

17. A method for controlling a solid state disk to write data, wherein the method is applied to a storage system, the storage system comprises an array controller and the solid state disk, the solid state disk comprises a flash memory chip and a solid state disk controller, and the flash memory chip comprises multiple blocks; and the method is performed by the solid state disk controller and comprises:

sending information about a logical block to the array controller, wherein the information about the logical block comprises a size of the logical block and indication information of the logical block, and the logical block comprises one or more blocks;

receiving multiple write data requests sent by the array controller, wherein each write data request includes target data, each write data request is used to instruct the solid state disk to write the target data into the logical block indicated by the indication information of the logical block, and a sum of lengths of the target data included in the multiple write data requests is equal to the size of the logical block; and

writing the target data included in each write data request into the logical block indicated by

the indication information.

18. The method according to claim 17, wherein the blocks comprised in the logical block are located in different channels.

19. The method according to claim 17 or 18, wherein the method further comprises:

determining that the logical block is in a to-be-written state, wherein the logical block in the to-be-written state indicates that the logical block has been allocated to store data; and

allocating the indication information to the logical block in the to-be-written state.

20. The method according to any one of claims 17 to 19, wherein the indication information of the logical block comprises an identifier of the logical block, and each write data request comprises the identifier of the logical block; and

the writing the target data included in each write data request into the logical block indicated by the indication information comprises: writing, according to the identifier of the logical block, the target data in each write data request into the logical block corresponding to the identifier.

21. The method according to any one of claims 17 to 19, wherein the indication information of the logical block comprises a logical address range of the logical block, and each write data request comprises a sub-range of the logical address range; and

the writing the target data included in each write data request into the logical block indicated by the indication information comprises: determining, according to the sub-range of the logical address range in each write data request and the logical address range of the logical block, the logical block corresponding to the target data in each write data request; and writing the target data in each write data request into the corresponding logical block.

22. The method according to any one of claims 19 to 21, wherein after the writing the target data into the logical block indicated by the indication information, the method further comprises reclaiming the indication information allocated to the logical block.

23. An apparatus for controlling a solid state disk to write data, wherein the solid state disk is located in a storage system, the solid state disk comprises a flash memory chip, the flash memory chip comprises multiple blocks, the storage system further comprises an array controller, and the apparatus is located in the array controller and comprises:

a receiving module, configured to receive information about a logical block sent by the solid state disk, wherein the information about the logical block comprises a size of the logical block and indication information of the logical block, and the logical block comprises one or more blocks; and

a processing module, configured to send multiple write data requests to the solid state disk, wherein each write data request includes target data, each write data request is used to instruct the solid state disk to write the target data into the logical block indicated by the indication information

of the logical block, and a sum of lengths of the target data included in the multiple write data requests is equal to the size of the logical block.

24. The apparatus according to claim 23, wherein the blocks comprised in the logical block are located in different channels.

25. The apparatus according to claim 23 or 24, wherein the logical block is in a to-be-written state, and wherein the logical block in the to-be-written state indicates that the logical block has been allocated by the solid state disk to store data.

26. The apparatus according to any one of claims 23 to 25, wherein the indication information of the logical block comprises an identifier that is allocated by the solid state disk to the logical block, and each write data request comprises the identifier of the logical block.

27. The apparatus according to any one of claims 23 to 25, wherein the indication information of the logical block comprises a logical address range that is allocated by the solid state disk to the logical block, and each write data request comprises a sub-range of the logical address range.

28. An apparatus for controlling a solid state disk to write data, wherein the solid state disk comprises a flash memory chip and a solid state disk controller, the flash memory chip comprises multiple blocks, and the apparatus is located in the solid state disk controller and comprises:

a transceiver module, configured to: send information about a logical block to an array controller, wherein the information about the logical block comprises a size of the logical block and indication information of the logical block, and the logical block comprises one or more blocks; and receive multiple write data requests sent by the array controller, wherein each write data request includes target data, each write data request is used to instruct the solid state disk to write the target data into the logical block indicated by the indication information of the logical block, and a sum of lengths of the target data included in the multiple write data requests is equal to the size of the logical block; and

a write module, configured to write the target data included in each write data request into the logical block indicated by the indication information.

29. The apparatus according to claim 28, wherein the blocks comprised in the logical block are located in different channels.

30. The apparatus according to claim 28 or 29, wherein the apparatus further comprises an allocating module, configured to: determine that the logical block is in a to-be-written state, wherein the logical block in the to-be-written state indicates that the logical block has been allocated to store data; and allocate the indication information to the logical block in the to-be-written state.

31. The apparatus according to any one of claims 28 to 30, wherein the indication information of the logical block comprises an identifier of the logical block, and each write data request

comprises the identifier of the logical block; and

the write module is specifically configured to write, according to the identifier of the logical block, the target data in each write data request into the logical block corresponding to the identifier.

32. The apparatus according to any one of claims 28 to 30, wherein the indication information of the logical block comprises a logical address range of the logical block, and each write data request comprises a sub-range of the logical address range; and

the write module is specifically configured to determine, according to the sub-range of the logical address range in each write data request and the logical address range of the logical block, the logical block corresponding to the target data in each write data request, and write the target data in each write data request into the corresponding logical block.

33. The apparatus according to any one of claims 30 to 32, wherein the allocating module is further configured to reclaim the indication information allocated to the logical block after the writing the target data into the logical block indicated by the indication information.