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SOLID STATE IMAGER DEVICES

This invention relates to solid state imager devices, and to methods of utilizing a solid state imager device as an electronic shutter, for example, for an electronic camera such as a video camera or an electronic still camera.

It has been required that a solid state imager device be able to control its exposure time by electronic means provided therein, so that when the imager device is used in, for example, a video camera, the use of a mechanical shutter as hitherto proposed, is unnecessary. Without a mechanical shutter, a video camera could be made smaller, lighter, and more cheaply.

There has already been proposed a solid state imager device which permits selection between two exposure times, one long and one short. This imager device has one of the two exposure times chosen to be 1/30 second, which is equal to one frame period in the NTSC television system, and the other exposure time chosen to be about 1/2000 second, which is equal to a vertical blanking period.

In this imager device, when the 1/30 second exposure time is selected, signal charges accumulated in the light receiving section during one frame period are read out as an image signal. On the other hand, when the 1/2000 second exposure time is selected, signal charges accumulated before a vertical blanking period are read out to a vertical register section and discharged by a high speed transfer, while signal charges newly accumulated only during the vertical blanking period are read out as an image signal.

However, this imager device is limited in that it only allows selection between two exposure times so that, even when a video camera is equipped with such an imager device, it still requires a mechanical shutter. Moreover, since a high speed transfer is required to discharge the signal charges accumulated before a vertical blanking period to the vertical register, the imager device consumes excessive electric power.

According to the present invention there is provided a solid state imager device comprising:

a semiconductor substrate of first conductivity type;

a region of second conductivity type formed on said substrate; and

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a signal charge accumulating region formed on a surface side of said second conductivity type region;

characterized by:

means for applying a predetermined voltage to said substrate thereby to discharge signal charges accumulated in said signal charge accumulating region to said substrate.

According to the present invention there is also provided a method of utilizing a solid state imager device as an electronic shutter for an electronic camera, comprising the step of applying voltage potential aeross a semiconductor substrate of a first conductivity type and a region of a second conductivity type formed on said substrate, thereby to discharge signal charges accumulated in a signal charge accumulating region formed on a surface side of said second conductivity type region to said substrate.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional view showing an embodiment of solid state imager device according to the present invention;

Figure 2 is a graph showing potentials of respective regions of the imager device of Figure 1 in the depth direction thereof;

Figures 3A and 3B are timing charts for explaining a shutter function of the imager device; and

Figures 4A to 4E are timing charts for explaining another shutter function of the imager device.

The solid state image device of Figure 1 comprises an N type silicon substrate 1 upon which a light receiving section 4, a vertical register section 5, a horizontal register section (not shown) and an output section (not shown) are formed, so as to constitute a so-called interline transfer charge coupled device (CCD) type imager device. On the surface of the substrate 1 there is deposited, for example, by epitaxial growth techniques, a P type region 2. An N^- type region 6 is deposited on the surface of the P type region 2.

The light receiving section 4 is formed of a shallow P^{++} type region 7 formed in a surface region of the N^- type region 6 and an N^+ type region 3 is formed beneath the P^{++} type region 7 to constitute a signal charge accumulating region. There is also a P^+ type region 8 constituting a channel stopper section formed adjacent

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to the P^{++} type region 7 and the N^+ type region 3. An insulating layer 9 made of SiO_2 is deposited on the P^{++} type region 7.

The vertical register section 5 is formed such that an N^+ type region 11, which constitutes a signal charge transfer region, is formed adjacent to a P type region 10, which constitutes a read-out gate region. A transfer electrode 13 made of polysilicon and another insulating layer 12 made of Si_3N_4 are formed above the N^+ type region 11 within the SiO_2 insulating layer 9. One end portion of the transfer electrode 13 is also used as a read-out gate electrode 13A. A P type region 14 is formed, for preventing smear, beneath the N^+ type region 11. An aluminium layer 15 for shielding light is deposited above the transfer electrode 13 above the insulating layer 9.

Although only two of the transfer electrodes 13 are illustrated in Figure 1, there are disposed a predetermined number of transfer electrodes 13 such that the vertical register section 5 is driven in known manner by a four-phase drive. The horizontal register section and the output section which are not illustrated in the drawing, are of known form.

In the embodiment of Figure 1, the negative voltage terminals of direct current (DC) power supply sources 16 and 17 are commonly connected to the P type region 2 and earthed. The positive voltage terminals of the sources 16 and 17 are connected to first and second fixed contacts 18A and 18B, respectively, of a switching circuit 18. A movable contact 18C of the switching circuit 18 is connected to the substrate 1.

An output voltage V_L from the source 16 is selected to be a value, for example, 10 volts, such that when the voltage V_L is applied to the substrate 1, the potential in the P type region 2 becomes slightly lower than the potential of the shallow P^{++} type region 7 on the surface of the N^+ type region 3, as shown by a solid line X in Figure 2, so that signal charges can be accumulated in the N^+ type signal charge accumulating region 3 and blooming can be effectively suppressed. An output voltage V_H from the source 17 is selected to be a value, for example 30 volts, such that when the voltage V_H is applied to the substrate 1, the potential in the P type region 2 becomes lower than the potential in the signal charge

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accumulating region 3, as is shown by a broken line Y in Figure 2, so that the signal charges accumulated in the signal charge accumulating region 3 can be discharged to the substrate 1. Switching of the switching circuit 18 can be controlled by a control signal supplied thereto through a control signal input terminal 19.

In this embodiment, when a read-out pulse P_2, as shown in Figure 3A, is supplied to the read-out gate electrode 13A while the output voltage V_L from the source 16 is applied to the substrate 1, signal charges accumulated in the signal charge accumulating region 3 are read out to the vertical register section 5. Therefore, in the present embodiment, the read-out pulse P_2 is supplied to the read-out gate electrode 13A at every field within the vertical retrace.

After the read-out pulse P_2 has been supplied to the read-out gate electrode 13A, if the switching circuit 18 is controlled so as to supply the substrate 1 with the 30 volts pulse, that is supplying a discharging pulse P_1 at a desired time within one field period as shown in Figure 3B, signal charges accumulated in the signal charge accumulating region 3 for a period t_2, that is a period from the time the proceeding read-out pulse P_2 is applied to the read-out gate electrode 13A to the time the current discharging pulse P_1 is applied to the substrate 1, are transferred to the substrate 1. Therefore, when the next read-out pulse P_2 is supplied to the read-out gate electrode 13A, signal charges accumulated in the signal charge accumulating region 3 for the period t_1, that is a period from the supply of the present read-out pulse P_2, are read out to the vertical register section 5.

As described above, the exposure time of the imager device becomes the period t_1, so that a desired exposure time can be obtained by selecting the time of supply of the discharging pulse P_1 to the substrate 1. Accordingly, when this imager device is used in a video camera, it does not have to be provided with a mechanical shutter, so that it is possible to reduce the size, weight and manufacturing cost of the camera.

Furthermore, for discharging the signal charges, the imager device does not have to operate the vertical register section 5 at a high speed as do the previously proposed solid state imager devices. The present imager device only requires, for example, a pulse of

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30 volts to be applied to the substrate 1, so that the electric power necessary for the exposure control can be substantially reduced.

With reference now to Figures 1 and 4A to 4E, another method for controlling the exposure time of the imager device will be explained.

In this method, after signal charges accumulated in the signal charge accumulating region 3 for the preceding field period have been read out by the read-out pulse P_2 shown in Figure 4A (the same as that shown in Figure 3A) to the vertical register section 5, the voltage V_H (30 volts) is applied from the source 16 through the switching circuit 18 to the substrate 1 so as to discharge the signal charges accumulated in the signal charge accumulating region 3 in such a manner that an arbitrary number of the horizontal blanking periods, each being set at 63.5 microseconds, are successively selected. During the horizontal blanking periods thus selected, the switching circuit 18 is controlled by the control signal applied thereto from the terminal 19 so that the movable contact 18C engages the second fixed contact 18B. In other words, after the signal charges have been read out by the read-out pulse P_2, the voltage V_H (30 volts) is applied to the substrate 1 at every horizontal blanking period to discharge the signal charges accumulated in the signal charge accumulating region 3 immediately before the exposure is started. During the exposure time period t_1 (Figure 4B), the voltage V_L (10 volts) is applied from the source 16 through the switching circuit 18 to the substrate 1 to accumulate signal charges in the signal charge accumulating region 3. Figure 4C shows a horizontal clock signal while Figure 4D shows a horizontal blanking signal, and Figure 4E shows the voltages to be applied to the substrate 1 within the horizontal blanking period.

With the method just described, the exposure time t_1 can be changed in a range between 1/60 and 1/10000 of a second by selecting the number of horizontal blanking periods for discharging the signal charges accumulated in the signal charge accumulating region 3, as shown in Figure 4B.

As described above, the exposure time is controlled by changing the voltage applied to the substrate 1. Since the voltage V_H is applied to the substrate 1 within the horizontal blanking period, even although a buffer amplifier and other devices forming the output

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section are caused to fluctuate by changing the voltage applied to the substrate 1, the reproduced image will not be influenced by the above change, so that it is possible to obtain reproduced images with a constant contrast.

The above description relates to where the signal charges are discharged at every horizontal blanking period immediately before the exposure is started. Apart from that, modifications can be made dependent on the characteristics of a solid state imager device such as where the signal charges are discharged only once within the horizontal blanking period and immediately before the exposure is started or where some of the horizontal blanking periods before the exposure is started are selected to discharge the signal charges. In other words, the number of discharges can be selected in accordance with the characteristics of each solid state imager device.

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CLAIMS

1. A solid state imager device comprising:
a semiconductor substrate (1) of first conductivity type;
a region (2) of second conductivity type formed on said substrate (1); and
a signal charge accumulating region (3) formed on a surface side of said second conductivity type region;
characterized by:
means (16 to 18) for applying a predetermined voltage to said substrate (1) thereby to discharge signal charges accumulated in said signal charge accumulating region (3) to said substrate (1).

2. An imager device according to claim 1 wherein said predetermined voltage is applied to said substrate (1) within a horizontal blanking period so as to cause the signal charges accumulated in said signal charge accumulating region (3) to discharge to said substrate (1) within the horizontal blanking period.

3. A method of utilizing a solid state imager device as an electronic shutter for an electronic camera, comprising the step of applying voltage potential across a semiconductor substrate (1) of a first conductivity type and a region (2) of a second conductivity type formed on said substrate (1), thereby to discharge signal charges accumulated in a signal charge accumulating region (3) formed on a surface side of said second conductivity type region (2) to said substrate (1).

4. A method according to claim 1 wherein said predetermined voltage is applied within a horizontal blanking period so as to cause said signal charges accumulated in said signal charge accumulating region (3) to discharge to said substrate (1) within said horizontal blanking period.

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