ABSTRACT

A METHOD FOR IMPROVED FABRICATION OF A SEMICONDUCTOR USING A STRESS PROXIMITY TECHNIQUE PROCESS

An improved method for applying stress proximity technique process on a semiconductor device and the improved device is disclosed. In one embodiment, the method utilizes an additional set of sidewall spacers on one or more NFET devices during the fabrication process. This protects the one or more of the NFET devices during the activation of a compressive PFET stress liner, thereby reducing the compressive forces on the one or more NFET devices, and creating a semiconductor device with improved performance.

Fig. 10