ELECTRONIC APPARATUS AND EXTERNAL APPARATUS USING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electronic apparatus that can be freely attached to and/or detached from an external apparatus and is suitable for enabling an apparatus for realizing an arbitrary function, and an external apparatus using the same. More specifically, relates to an electronic apparatus having a shape, for example, equivalent to a memory card apparatus or a similar semiconductor memory apparatus, such electronic apparatus executing an arbitrary operation upon being connected to a connecting portion of the external apparatus, and the external apparatus using the electronic apparatus.

2. Related Art

It is proposed an electronic apparatus having a shape equivalent to a memory card apparatus that can be freely attached and/or removed as against an external apparatus or a similar semiconductor memory apparatus, executing an arbitrary operation upon being connected to a connecting portion of such memory apparatus of the external apparatus. In other words, it is possible to easily expand the utility or application of an external apparatus by making such electronic apparatus have, for

example, a computer network connecting function or an external communication function.

However, when utilizing such electronic apparatus connected to an external apparatus, the amount of power consumption of the external apparatus inevitably increases, so that an internal battery thereof is consumed in a short term as a result of such increase in power consumption, consequently making it difficult to have a long-term utilization by applying the battery. Such increase in power consumption is particularly remarkable when the electronic apparatus has multiple functions. As a result, a an electronic apparatus conventionally has only one function, therefore making operations inconvenient as the electronic apparatus has to be changed every time a new function is required.

In view of such problem, it is possible to conceive a case in which while multiple functions are provided to an electronic apparatus, a means for controlling power supply from the outside is also provided so that controlling is done so as to supplying power only to a required function. However, such methodology is difficult to realize as it increases the load of the external apparatus as complex procedures are required for controlling the external apparatus, such as requiring controlling of individual power supply each time a function is selected from the external apparatus.

SUMMARY OF THE INVENTION

The present invention has been conceived in view of such problems, that is, when using a conventional apparatus by attaching an electronic apparatus of multiple functions to an external apparatus, a long term utilization through a battery is difficult to realize as the internal battery is consumed in a short term as a result of the increase in power consumption due to presence of the multiple functions. In addition, when controlling power supply from the external apparatus each time a function is selected, the processing required for the external apparatus becomes complicated.

In accordance with a first aspect of the present invention, there is provided an apparatus being coupled to a host system, the apparatus receiving electric power from the host system and performing a function, comprising:

a plurality of function blocks, and

a circuit for reducing the amount of power consumption of a function block which is not selected from the plurality of function blocks by the host system.

In accordance with a second aspect of the present invention, there is provided an apparatus being coupled to a host system, the apparatus receiving electric power from the host system and performing a function, comprising:

a plurality of function blocks;

a circuit for reducing the amount of power consumption of a function block which is not selected from the plurality of function blocks; and

a register which is common to the plurality of function blocks, wherein

the register stores a function code which indicates a function block selected by the host system and a power save value which indicates that a power save mode is selected by the host system, and

the circuit for reducing the amount of power consumption reduces the amount of power consumption of a function block whose function code is not stored in the register when the power save value is stored in the register.

In accordance with a third aspect of the present invention, there is provided a data processing system comprising an apparatus and a host system, the apparatus receiving electric power from the host system and performing a function, the apparatus comprising:

a plurality of function blocks;

a function register which is common to the plurality of function blocks and stores a function code which indicates a function block selected by the host system; and

a circuit for reducing the amount of power consumption; wherein

the circuit reduces the amount of power consumption of a function block whose function code is not stored in the function register; and

the host system comprises a means for writing the function code into the function register.

In accordance with a fourth aspect of the present invention, there is provided a data processing system comprising an apparatus and a host system, the apparatus receiving electric power from the host system and performing a function, the apparatus comprising:

a plurality of function blocks;

a circuit for reducing the amount of power consumption of a function block which is not selected from the plurality of function blocks; and

a register common to the plurality of function blocks; wherein

the register stores a function code which indicates a function block selected by the host system and a power save value which indicates that a power save mode is selected by the host system; and

the circuit for reducing the amount of power consumption reduces the amount of power consumption of a function block whose function code is not stored in the register when the power save value is stored in the register.

In accordance with a fifth aspect of the present invention, there is provided a method of controlling an amount of power consumption of an apparatus which receives electric power from a host system and comprises a

register and a circuit for reducing the amount of power consumption, the method comprising the following steps of:

(a) the host system starting supplying electric power to the apparatus in a standby mode;

(b) the host system selecting a function block from the plurality of function blocks;

(c) the host system sending a function code which indicates a selected function block to the apparatus;

(d) the apparatus setting the function code to the register; and

(e) the circuit of the apparatus reading the function code from the register and reducing the amount of power consumption of a function block whose function code is not stored in the register.

According to a preferred embodiment of the present invention, a means for reducing the power consumption when a function block is not selected is provided for the electronic apparatus and, as a result, it is possible to reduce the power consumption by reducing the power consumption of the electronic apparatus to the minimum required through a simple structure. Accordingly, it is possible to utilize the internal battery for an extended period of time and also without increasing the burden of processing at the external apparatus.

According to another embodiment of the present invention, it is possible to change over functions through a simple structure in which it is enough just to change the content of a setting register according to selection of a function block of the electronic

apparatus, such selection determined by writing related data into a function register.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the present invention will be apparent to those skilled in the art from the following description of the presently preferred exemplary embodiments of the invention taken in connection with the accompanying drawings, in which:

FIG. 1 is a block diagram of an electronic apparatus and an external apparatus according to a preferred embodiment of the present invention;

FIG. 2 is an outline view of an electronic apparatus according to a preferred embodiment of the present invention;

FIG. 3 is a table describing the electronic apparatus according to the preferred embodiment of the present invention;

FIG. 4 is another table describing the electronic apparatus according to the preferred embodiment of the present invention;

FIG. 5 is another table describing the electronic apparatus according to the preferred embodiment of the present invention; and

FIG. 6 is a flowchart describing an operation of the electronic apparatus according to the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to a preferred embodiment of the present invention, there is proposed an electronic apparatus performing an arbitrary function, that can be freely attached/detached as against an external apparatus, while performing exchange of arbitrary data with the external apparatus; such electronic apparatus has a plurality of function blocks plus a means for turning down power consumption during application of power and for a function block that is not selected.

In addition, according to another preferred embodiment of the present invention, there is proposed an external apparatus using an electronic apparatus for performing an arbitrary function, to which the electronic apparatus can be freely attached/detached, while performing exchange of arbitrary data with the electronic apparatus; such electronic apparatus has a means for writing information regarding utilization on a function register common to a plurality of function blocks provided in the electronic apparatus, as well as a means for writing set up data of an arbitrary function on a designated register corresponding to the function block determined as selected according to the information written in the function register.

The preferred embodiments of the present invention are explained below with reference to the drawings, in which FIG. 1 represents an electronic apparatus according to a preferred

embodiment of the present invention, as well as a structure of an external apparatus constituting another preferred embodiment of the present invention using the electronic apparatus.

The left portion of FIG. 1 shows as an external apparatus using the electronic apparatus, an external apparatus 100 such as, for example, a personal computer. Such external apparatus 100 is provided with a media controller 12 connected to a system bus 11 and, in such media controller 12, there is provided, for example, a camera controlling protocol circuit 13, a GPS(Global Positioning System: a satellite-based positioning system) controlling protocol circuit 14 and an interface 15 connected to the electronic apparatus.

On the other hand, the left portion of FIG. 1 shows an electronic apparatus 200. Such electronic apparatus 200 has a configuration similar to a so-called memory card apparatus as shown in FIG. 2, or a semi-conductor memory apparatus of similar type. In addition, while being able to be freely attached/detached from a memory card slot of the external apparatus 100, the electronic apparatus 200 can be electrically connected to the interface 15 of the media controller 12 of the external apparatus 100 via a connector cluster 201 formed on an end thereof.

In addition, the electronic apparatus 200 is provided with a plurality of functions. As far as the present preferred

embodiment as one of several possible embodiments of the present invention is concerned, there is provided, for example, a GPS function block 21 as a function A, a camera shooting function block 22 and a memory function block 23 as a function B. Moreover, such function blocks 21 to 23 are connected to an interface 24 connected to the connector cluster 201 mentioned above via a register 300, thus permitting exchange of data between the external apparatus 100.

Furthermore, for each of the function blocks 21 and 22 there is provided respective power controlling portions 21a and 22a. In addition, a power-control signal from a system controlling circuit 25 connected to the register 300 is supplied to the power controlling portions 21a and 22a. As a result, by providing such an electronic apparatus 200 that can be freely attached/detached against the external apparatus 100, it is possible to supply power between the media controller 12 of the external apparatus 100 and the register 300 of the electronic apparatus 200, as well as exchanging data through a data buffer 26.

In addition, the register 300 is provided for the system including the external apparatus 100 and the electronic apparatus 200. Such register 300 includes, for example, addresses from "00" to "FF" ("- -" indicates an hexadecimal number), and both a read out register and a write register of 2

bytes each are provided for each address. To the read out register, information contained inside the electronic apparatus 200 is read out, while to the write register, information from the external apparatus 100 is written.

First of all, an address structure of a memory function of the register 300 is shown in FIG. 3. That is, in FIG. 3, address "00" is not used, while a read out register of address "01" is a interrupt register and a read out register of address "02" and "03" is a status register. Furthermore, write registers of addresses "01" to "03" are not used, while both read out and write registers of address "04" are type registers. In addition, address "05" is not used.

Moreover, the read out and the write registers of address "06" are category number registers that show a function to be executed inside the electronic apparatus 200. In addition, the read out register of address "07" is a class number register, while the write register of address "07" is not used. Furthermore, the read out register of address "08" is a current request register, while the write register thereof is a function validation register.

In addition, the read out register of addresses "09" and "0A" are registers for attribute information length. Attribute information is stored in an attribute ROM 27 inside the electronic apparatus 200 and, when the electronic apparatus has a memory function that enables writing, such attribute information is read

out from the attribute ROM 27 and stored into the memory function described above, at the time of factory delivery. As a consequence, for an ordinary communication other than at the time of factory delivery, attribute information stored in the memory function is read out and access to the attribute ROM 27 is forbidden. Nevertheless, when the electronic apparatus does not have a memory function, the attribute information stored in the attribute ROM 27 is read out by the host, even for an ordinary access.

Still further, the write register of address "10" is a system parameter register, while the write register of addresses "11" to "13" is a block address register. Still, the write register of address "14" is a command parameter register. In addition, the read out register of addresses "10 " to "14" are not used. Moreover, the read out register and the write register of address "15" are page address registers.

In addition, the read out register and the write register of address "16" are block flag data registers. Further, the read out register and the write register of address "17" are block information registers. In addition, the read out registers and the write registers of addresses "18" and "19" are logic address registers. Moreover, a format for addresses "1A" to "1F" is currently under process of formulation.

On the other hand, an address structure for the GPS function is as shown in FIG. 4. Furthermore, the GPS function block has a GPS antenna for receiving positioning information and a GPS function controller. The GPS controller includes units such as a UART (Universal Asynchronous Receiver-Transmitter), a FIFO (First In First Out Buffer) and a power controlling unit. In other words, structures of addresses from "00" to "0F" in FIG. 4 are the same as for the memory function. In addition, as for the GPS function, addresses from "10" to "15" have access disabled.

Moreover, addresses from "16" to "17" are not used. Further, the read out register and the write register of address "18" are registers for setting transmission speed of information data between the external apparatus 100 and the electronic apparatus 200. In addition, address "19" is a register showing a status of a Universal Asynchronous Receiver-Transmitter (hereinafter referred to simply as UART), which performs change of a digital data signal transmitted and received through an antenna, from serial to parallel, or vice-versa.

In addition, the read out register of address "1A" is a register showing a volume of data remaining in a First In First Out (hereinafter referred to simply as FIFO) memory at the receiving side, which buffers a difference in data transmission speed, while the read out register of address "1B" is a register

showing a volume of free buffer space of the FIFO at the transmitting side. Moreover, the write register of address "1A" is a data length register of data received from the external apparatus 100, while the write register of address "1B" is a data length register of data sent to the external apparatus 100.

In addition, the write register of address "1C" is a register for generating interrupt when the volume of data accumulated in the FIFO memory at the receiving side reaches a designated number of bytes, while the write register of address "1D" is a register for generating interrupt when the volume of data accumulated in the FIFO memory at the transmitting side is below a preset value. Furthermore, in any case, the value "0" is invalid. In addition, the read out registers of both addresses "1C" and "1D" are not used.

In addition, the read out registers of addresses "1E" and "1F" are registers showing clock values of UART, while the write registers thereof are not used. Furthermore, the read out register and the write register of address "20" are registers for controlling/monitoring respective universal digital I/O terminals provided on the electronic apparatus 200. Moreover, addresses "21" to "2F" are in a stage of having their formats designed. The settings for the GPS function are thus set as above, as an example.

Moreover, an address structure for a camera function can be set as shown, for example, in FIG. 5. It is to be understood that the camera function block includes a shooting unit having, for example, a lens or a CCD for receiving shooting light coming from an object of shooting, as well as a camera function controller. The camera function controller includes a power controlling unit, a shooting signal processing unit and the like. As a result, the structures of addresses from "00" to "0F" in FIG. 5 are similar to the structure for the memory function. In addition, as for the camera function, addresses from "10" to "15" have access disabled.

Moreover, addresses "16" and "17" are not used. Also, the read out register and the write register of address "18" are registers for controlling the camera. Furthermore, the read out register of address "19" is a register for length of data received from the external apparatus 100, while its write register is a register for length of data sent to the external apparatus 100.

In addition, the camera function controller, the GPS function controller and the memory function controller have each their own power controlling functions controlled by a power controlling unit of a system controlling circuit and, when not used, such function is set to a sleeping mode (a status in which a controller clock is stopped), thus reducing power consumption. Furthermore, this may apply to an arbitrary information apparatus, an apparatus for connecting to a network (e.g., LAN)

of a designated range (e.g., Ethernet) or the like, an arbitrary modem apparatus, a communication apparatus commonly recognized by Japanese, American and European (such as a Bluetooth compatible apparatus) or the like, or an arbitrary serial communication function or the like.

Moreover, when, for example, changing over a function to be performed by the electronic apparatus 200 through the external apparatus 100, first a desired function code (a category number) is written into the write register of the address "06" mentioned above. Accordingly, the function code (category number) written into such write register of address "06" is read out to the system controlling circuit 25 of the electronic apparatus 200, whereby a function requested from the external apparatus 100 can be recognized by the electronic apparatus 200.

In addition, a control signal for activating, for example, the function block 21 or the function block 22 is formed in the system controlling circuit 25, in order to make such recognized function be executed by the electronic apparatus 200. In other words, the address structure of register 300 is changed over according to the recognition mentioned above. Moreover, the function requested by the external apparatus 100 is performed by the electronic apparatus 200 by providing the control signal formed in the system controlling circuit 25 using such register 300 to each of

respective power control units 21A and 22A of function blocks 21 or 22.

Furthermore, a class number related to, for example, version of a function performed by the electronic apparatus 200 is read out to the read out register of address "07", along with reading out a function code (a category number) of a function performed by the electronic apparatus 200 to the read out register of address "06". Moreover, by recognizing this category number and the class number at the external apparatus 100, a function to be performed by the electronic apparatus 200 in recognized, thus a driver or the like is activated accordingly, at the external apparatus 100.

The change over of a function to be performed by the electronic apparatus 200 is, therefore, done by, for example, writing a code related to a desired function (a category number) from the external apparatus to the write register of address "06". Then, by reading out the function code (category number) related to the function to be performed by this electronic apparatus 200 to the read out register of address "06", the function to be performed by the electronic apparatus 200 is recognized by the external apparatus 100, thereby allowing a smooth change over of functions.

In other words, if, for example, a function written from the external apparatus 100 into the write register of address "06" is

not available at the electronic apparatus 200, as the function code (category number) cannot be read out to the read out register of address "06", it is recognized by the external apparatus 100 that the desired function is not available at the electronic apparatus 200. As a result, a procedure like a discontinuation of such function by the external apparatus can be performed smoothly.

In addition, an action such as the one shown in a flowchart of FIG. 6 can be performed as against such system including the external apparatus 100 and the electronic apparatus 200. In other words, in FIG. 6, upon applying power to the external apparatus 100's side in step [11], the electronic apparatus 200's side goes to step [21]. Then, at such step [21], only the system controlling circuit 25 is turned to active mode, while a function A of function block 21 and the function B of function block 22 is turned to a stanby mode.

On the other hand, if a command for using the function A is issued at the external apparatus 100's side in step [12], the electronic apparatus 200's side turns to step [22], in which the function A operates as the function block 21 is activated. In addition, if a command for using the function B is issued at the external apparatus 100's side in step [13], the electronic apparatus 200's side turns to step [23]. Then, in such step [23], the function B operates as the function block 22 is activated,

while the function block 21 of function A is turned to standby mode.

In addition, if the command for using the function A is issued again at the external apparatus 100's side in step [14], the electronic apparatus 200's side turns to step [24]. Then, in such step [24], the function A operates as the function block 21 is activated, while the function block 22 of function B is turned to standby mode. By proceeding like that, a function A or B can be each performed as desired at the electronic apparatus 200's side, according to issue of a command at the external apparatus 100's side, for using either the function A or B.

Moreover, as for such operations, in step [21] mentioned above, supposing that, for example, an amount of electric current consumed by block 21 and 22, for instance, during standby mode is 10mA each and the amount of electric current consumed by the system controlling circuit 25 is 30mA, then the amount of electric current consumed by the electronic apparatus 200 is

$$10 + 10 + 30 = 50\text{mA}$$

On the other hand, as for steps [22] and [24], supposing that, for example, an amount of electric current consumed by block 21 during operation mode is 100mA, the amount of electric current consumed by the electronic apparatus 200 is

$$100 + 10 + 30 = 140\text{mA}.$$

In addition, in step [23], if , for example, the amount of electric current consumed by function block 22 during operation mode is 60mA, , the amount of electric current consumed by the electronic apparatus 200 is

10 + 60 + 30 = 100mA.

In other words, considering the system including the external apparatus 100 and the electronic apparatus 200, the amounts of electric current consumed at the electronic apparatus 200's side are, respectively, 50mA at step [21], 140mA at steps [22] and [24], and 100mA at step [23]. This is a small amount of current consumption, when compared to a case in which the function blocks 21 and 22 are both in the operation mode, thus having

100 + 60 + 30 = 190mA.

In addition, in such case, it is possible for the external apparatus 100 to establish power control over each of function blocks 21 and 22 by simply writing data onto register 300 of the electronic apparatus 200. Also, it is possible to establish power control over the function blocks 21 and 22 from the electronic apparatus 200 by looking at data contained in the register 300, thus constituting an extremely simple structure, which permits establishment of easy power control.

In addition, such values of electric current consumed are indicated, for example, in the read out register of address "08" as

a current request from the electronic apparatus 200's side. The read out register of address "08" is read out by the external apparatus 100 and, upon deciding whether such requested current is within an acceptable range, a function validation flag is set to the write register of the same address "08". As a result, it is possible to perform only a function that can be activated by the electronic apparatus 200. Moreover, the least significant bit of the write register is a power saving bit, thus by writing 1 to such bit, a power saving mode is set and, by writing 0 thereon, the power saving mode is released.

In addition, as the register 300 is conventionally provided for performing settings for each of function blocks 21 and 22 from the external apparatus 100, the preferred embodiment of the present invention makes a portion of this register 300 available for common use and establishing the address "06" as the function register, while allowing performance of a smooth setting of each function through its easy structure, as the address structure of a register to be set can be changed over for each function.

Accordingly, in the preferred embodiments of the present invention described above, by providing at the electronic device a means for reducing the power consumption of a function block when such block is not selected, the power consumption of the electronic device can be reduced to a minimum necessary by a simple structure, thus controlling an increase in power

consumption, and while permitting an extension of hours of use of an internal battery, the external apparatus does not have to cope with a burden of additional processing.

In a conventional apparatus, when using an electronic apparatus having a plurality of functions that is attached to an external apparatus, an internal battery thereof is consumed in a relatively short period of time as the power consumption increases dues to the plural functions thereof, thus making it difficult to operate for an extended time utilizing the battery. In addition, the preferred embodiments of the present invention permits a easy solution for the problem in the related art, namely, of controlling power supply for each selected function from the external apparatus, that is not easy to realize as a burden of processing increases for the external apparatus.

Furthermore, although in the preferred embodiments of the present invention selection of functions is described for a choice of 2 between A and B, a selection among 3 or more choices are also possible. In such case, it is possible to establish a plurality of functions to be selected accordingly. Conversely, if it is desired to limit utilization of a function block to exclusively 1 at a time, this can be easily set by just indicating the selected function from the external apparatus, through performing a procedure of reducing the power consumption of functions other than the one that has been selected.

Moreover, according to the preferred embodiments of the present invention, as an electric current flowing between the external apparatus and the electronic apparatus can be reduced, it is possible to utilize inexpensive specifications such as endurance specs for connectors, terminals or the like.

Finally, the configurations and structures of respective units and portions described specifically with respect to the preferred embodiments of the present invention are only examples of realization of the present invention, so the embodiments thereof should not be construed as to limiting the technical scope of the present invention.

Accordingly, the present invention is not limited to the preferred embodiments described above, thus any variation as well as any combination and/or sub combination of the embodiments is permitted, without departing from the scope of the present invention.

What is claimed is:

1. An apparatus being coupled to a host system, the apparatus receiving electric power from said host system and performing a function, comprising:

a plurality of function blocks, and

a circuit for reducing the amount of power consumption of a function block which is not selected from said plurality of function blocks by said host system.

2. The apparatus according to claim 1, further comprising:

a function register which is common to said plurality of function blocks and stores a function code which indicates a function block selected by said host system, wherein

said circuit for reducing the amount of power consumption reduces the amount of power consumption of a function block whose function code is not stored in said function register.

3. An apparatus being coupled to a host system, the apparatus receiving electric power from said host system and performing a function, comprising:

a plurality of function blocks;

a circuit for reducing the amount of power consumption of a function block which is not selected from said plurality of function blocks; and

a register which is common to said plurality of function blocks, wherein

said register stores a function code which indicates a function block selected by said host system and a power save value which indicates that a power save mode is selected by said host system, and

said circuit for reducing the amount of power consumption reduces the amount of power consumption of a function block whose function code is not stored in said register when said power save value is stored in said register.

4. A data processing system comprising an apparatus and a host system, the apparatus receiving electric power from said host system and performing a function, said apparatus comprising:

a plurality of function blocks;

a function register which is common to said plurality of function blocks and stores a function code which indicates a function block selected by said host system; and

a circuit for reducing the amount of power consumption; wherein

said circuit reduces the amount of power consumption of a function block whose function code is not stored in said function register; and

said host system comprises a means for writing said

function code into said function register.

5. A data processing system comprising an apparatus and a host system, the apparatus receiving electric power from said host system and performing a function, said apparatus comprising:

a plurality of function blocks;

a circuit for reducing the amount of power consumption of a function block which is not selected from said plurality of function blocks; and

a register common to said plurality of function blocks; wherein

said register stores a function code which indicates a function block selected by said host system and a power save value which indicates that a power save mode is selected by said host system; and

said circuit for reducing the amount of power consumption reduces the amount of power consumption of a function block whose function code is not stored in said register when said power save value is stored in said register.

6. The data processing system according to claim 5, wherein said host system comprises a means for writing said function code and said power save value into said register.

7. A method of controlling an amount of power consumption of an apparatus which receives electric power from a host system and comprises a register and a circuit for reducing the amount of power consumption, the method comprising the following steps of:

(a) said host system starting supplying electric power to said apparatus in a standby mode;

(b) said host system selecting a function block from said plurality of function blocks;

(c) said host system sending a function code which indicates a selected function block to said apparatus;

(d) said apparatus setting said function code to said register; and

(e) said circuit of the apparatus reading said function code from said register and reducing the amount of power consumption of a function block whose function code is not stored in said register.