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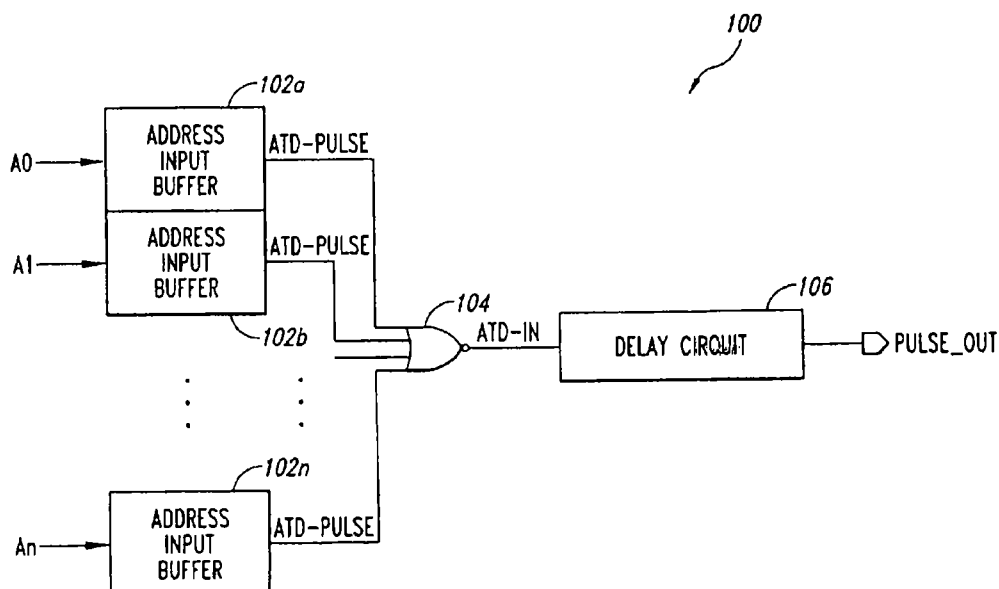
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- (71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 South Federal Way, Boise, ID 83716-9632 (US).
- (72) Inventors: **LOVETT, Simon, J.**; 13274 West Passage Court, Boise, ID 83713 (US). **ZITLAW, Cliff**; 3491 Suncrest Avenue, San Jose, CA 95132 (US). **SHIRLEY, Brian, M.**; 2484 Sunshine Drive, Boise, ID 83712 (US). **NORWOOD, Roger, D.**; 900 Hills Creek Drive, McKinney, TX 75070 (US). **SCHRECK, John, F.**; 29 White Rock Trail, Lucas, TX 75002 (US).
- (74) Agents: **ENG, Kimton, N.** et al.; Dorsey & Whitney LLP, 1420 Fifth Avenue, Suite 3400, Seattle, WA 98101 (US).
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(54) Title: ASYNCHRONOUS INTERFACE CIRCUIT AND METHOD FOR A PSEUDO-STATIC MEMORY DEVICE



(57) **Abstract:** An asynchronous address interface circuit (100) and method for converting unrestricted randomly scheduled address transition of memory address signals into scheduled address events from which initiation of a sequence of memory access events can be based. The address interface circuit initiates a delay sequence (106) based on an address transition detection pulse. In the event a new address transition detection pulse is received prior to completion of the delay sequence, the delay sequence (106) is reset and restarted on the new address transition detection pulse. The sequence of memory access events is initiated in response to the completion of the delay sequence.

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