

Description

The invention relates to a thin film transistor and crossover structure for a liquid crystal display device, including the features mentioned in the preamble of claim 1, and to a method for making such transistor and structure including the features listed in the preamble of claim 6.

Liquid crystal display devices include an array of liquid crystal elements (pixels) arranged in a matrix of rows and columns. In active matrix display devices, each pixel is associated with a solid state switching device, such as a thin film transistor (TFT). As is known in the art, a liquid crystal element is composed of a liquid crystal material arranged between two electrodes. The light transmission capability of the liquid crystal material is changed by voltage-biasing the electrodes to change the orientation of the molecules within the liquid crystal material. The liquid crystal elements are arranged in rows and columns, and individual elements are addressed by simultaneously voltage-biasing a drive line and a data line which are individually coupled to the electrodes of the elements. The biasing voltage to one of the electrodes of the liquid crystal element is applied through a solid state switching device (TFT) to enable the liquid crystal elements to store a charge for the time required to produce a visual display. Accordingly, the fabrication of a liquid crystal display device includes the fabrication of the TFT's and the connection of the TFT's to the control electrodes of the liquid crystal elements.

Published French application FR-A-2602361 discloses thin film transistor and crossover structure for a liquid crystal display device comprising a transparent substrate supporting a transparent electrode layer which is configured into pixel electrodes, drive lines and data lines. A doped layer is provided over selected portions of said transparent electrode layer for forming source and drain regions for said thin film transistor. Over said doped layer there is an undoped layer for forming a channel region between said source and drain regions. A dielectric layer over said undoped layer forms a gate electrode for said thin film transistor, and a first conductive layer over selected portions of said dielectric layer makes electrical contacts to said pixel electrode, said drive lines and said data lines. A second conductive layer over selected portions of said first conductive layer is in electrical connection therewith for forming electrode crossovers and for connecting said pixel electrodes to drive circuitry. US-A-4,680,085 which is also concerned with a thin film semiconductor device, relates to a provision of an edge dielectric coating.

Typically, in the fabrication of TFT's for liquid crystal displays, various photographic masks are

employed whereby different portions of the TFT's and the liquid crystal electrodes are formed at various steps in the process. Also typically, the number of masks used in fabricating the TFT's is four. However, as is known, the yield of devices fabricated using multiple masks varies inversely with the number of masks used. Accordingly, it is advantageous to decrease the number of masks used in the formation of the TFT's. In keeping with this goal, it is possible to fabricate the TFT's for liquid crystal display devices utilizing only two masks. The two-mask process is advantageous when the drive circuitry used to energize the drive and data lines is fabricated separately from the solid state switching devices of the liquid crystal display. However, it should be appreciated that a substantial cost saving can be realized by simultaneously fabricating the TFT's and the drive circuitry onto the substrate which supports the liquid crystal matrix. The two-mask processing has several disadvantages when the drive circuitry is to be so fabricated. Firstly, a parasitic transistor is formed and connects the pixel transistors to the data line; this parasitic transistor can deleteriously affect the on/off characteristics of adjacent TFT's or can cause crosstalk between adjacent data lines. Another disadvantage is that the data lines have a high resistance. Yet another disadvantage is the lack of an electrical connection between the gates of the TFT's and the source or drain lines.

The object of the invention is provision of a cost-saving thin film transistor and crossover structure for a liquid crystal display device which does not suffer from parasitic transistors and high data line resistance and allows electrical connection between the gates of the thin film transistors and the source and drain lines. A further object is to provide for a low cost method for making such transistor and crossover structures.

These objects are being solved by the characterizing features of claims 1 and 6, respectively, whereby particular embodiments of the inventions are included in the subclaims.

In accordance with present invention, a thin film transistor (TFT) and crossover structure for a liquid crystal display device includes a transparent electrode layer supported by a transparent substrate. The transparent electrode layer is configured into pixel electrodes, drive lines and data lines. A doped layer over selected portions of the transparent electrode layer forms source and drain regions for the TFT. An undoped layer over the doped layer forms a channel region between the source and drain regions. A dielectric layer over the undoped layer forms a gate electrode for the TFT. A first conductive layer over selected portions of the dielectric layer makes electrical connections to the pixel electrode, the drive lines and the data

lines. A second conductive layer over selected portions of the first conductive layer is in electrical connection with the first conductive layer and with portions of the transparent electrode layer, to form electrode crossovers and to connect the pixel electrode to drive circuitry. The present invention provides a three-mask process which permits the interconnection of the gate and source/drain regions of various transistors. The invention also provides a crossover structure which enables the drive circuitry to be fabricated on the same substrate as the display device. Another advantage is the provision of a dielectric stringer which inhibits the formation of a parasitic resistor between the gate and channel regions of the TFT's.

In the drawings:

FIGURES 1a to 1e sequentially show the steps of a preferred three-mask process for fabricating a preferred embodiment of the TFT.

FIGURE 2 shows the connection of the TFT to the control electrode of a liquid crystal element.

FIGURE 3 is another preferred embodiment of the TFT.

FIGURE 4 is an example of peripheral circuitry which can be simultaneously fabricated along with the TFT's of a liquid crystal display device.

FIGURE 5 is the equivalent circuit of the structure of FIGURE 4.

FIGURES 1a to 1e sequentially show a three mask process for forming TFT's and a crossover structure for a liquid crystal display device. In these figures, the apparent crosshatching is not intended as such. Each layer is shaded differently, and the various layers are similarly shaded in all the figures, to facilitate the visual identification of the various layers. The shadings which identify the various layers are shown in the legend which appears below FIGURE 1e.

In FIGURE 1a, one surface of a transparent substrate 11 is coated with a transparent electrode layer 12. In FIGURE 1b, a doped layer 13, which preferably is doped amorphous silicon, is deposited over the transparent electrode layer 12. FIGURE 1c shows how selected areas 14, 15 and 16 remain after the first mask is used in a photographic and etching process, to remove the portions of the transparent electrode layer 12 and amorphous silicon layer 13 which are not needed to form the device. In FIGURE 1d, an undoped layer 17, which preferably is undoped amorphous silicon, is deposited over the entire structure. The undoped layer 17 thus extends between the portions 14 and 15 and serves as a channel region between the portions 14 and 15, which respectively function as the source and drain regions of a TFT. A dielectric layer 18 is deposited over the entire undoped amorphous silicon layer 17. The dielectric layer 18 serves as the gate layer for the TFT. A

first conductive layer 19, which preferably is metal, is deposited over the entire dielectric gate layer 18. Many techniques for depositing the layers 17, 18 and 19 onto the substrate 11 are known per se. The second mask of the three-mask procedure is used to remove selected portions of the layers 13, 17, 18 and 19. In FIGURE 1e, a second conductive layer 21, which also preferably is metal, is deposited over selected portions of the device utilizing the third mask of the procedure. As shown in FIGURE 1e, the second conductive layer 21 extends between the drain portion 15 of the TFT and the portion of the electrode layer 12 which serves as the control electrode for the liquid crystal device. Some portions, such as 21a, of the second metal layer 21 are insulatively spaced from the conductive electrode layer 12, so that effective crossover structures are available. Additionally, other portions, such as 21b, of the second metal layer 21 contact the conductive electrode layer 12 and thus are available for connecting selected portions of the conductive electrode layer 12 to external drive circuitry, or to output devices.

FIGURE 2 shows a portion of a liquid crystal display device which can be fabricated using the inventive method. Various conductors 22, 22a and 23 are formed from the transparent electrode layer 12. Conductor 22 is the control electrode for a liquid crystal cell. Conductor 22a is an extension of control electrode 22 and connects electrode 22 to the drain 24 of a TFT, which also includes a source 28 and a channel 31. The conductor 23 passes under a conductor 27, which is formed from the first and second metal layers 19 and 21. The widths of layers 19 and 21 are different for illustration purposes; in an actual device, they are very nearly the same width. The conductor 23 is separated from conductor 27 by layers 13, 17 and 18 and thus forms crossover 30. Crossover 30 permits the connection of conductor 27 to drive circuitry 32, which is also fabricated when the TFT and crossover 30 are fabricated. The source 28 of the TFT is formed where another portion 29 of transparent electrode 12 passes under conductor 27. A channel 31 of the TFT connects source 28 and drain 24 of the TFT; in FIGURES 1d and 1e, this is illustrated where layer 17 connects source 14 and drain 15. Because of the ability to form crossovers, such as crossover 30, the data lines and drive lines needed to actuate control electrode 22 can be simultaneously fabricated along with the TFT's, the other conductors and drive circuitry 32. Substantial savings in fabrication cost and a significant increase in yield are thereby realized.

A problem can occur with the process as described with respect to FIGURES 1a through 1e. As shown in FIGURE 1e, when the second conductive layer 21 is applied to the device, the metal con-

tacts the edges of the undoped amorphous silicon layer 17 and the dielectric gate layer 18. This can result in a parasitic resistor between the gate and channel regions of the transistor. The resistance of this resistor can be quite high. However, problems can nevertheless arise under certain circumstances. FIGURE 3 shows a solution to the problem of parasitic resistance. Dielectric stringers 33 are formed over the exposed amorphous silicon edges, to prevent the second metal layer 21 from contacting the edges of the undoped amorphous silicon layer 17. The stringers 33 are formed by depositing a dielectric layer over the entire surface of the device and anisotropically removing the layer from the planar surfaces using a plasma-etch system. The dielectric layer is inherently thicker along the edges of the layers than it is over the planar surface of the layer and, therefore, is not completely removed along the edges during the stripping process. The stringer formation therefore requires only a deposition and an etch step; a photography step utilizing a mask is not required.

FIGURE 4 shows an exemplary drive circuit which can be fabricated along with the TFT's and electrodes of a liquid crystal display device utilizing the claimed method. A plurality of transparent conductors 34, 35, 36 and 37 are formed from the electrode layer 12 of FIGURE 1a. Another plurality of conductors 38, 39, 40 and 41 are formed from the second conductive layer 21 of FIGURE 1e. Another set of conductors 42, 43 and 44 are formed from the first conductive layer 19 of FIGURES 1d and 1e. Conductor 38 is electrically connected to conductors 34 and 42. However, conductors 34 and 35 are partially beneath conductor 42 and are electrically insulated from conductor 42 by layers 17 and 18 of FIGURE 1e to thereby form a TFT 45, the drain of which is electrically connected to conductor 34, and the source of which is electrically connected to conductor 35. Conductor 39 is electrically connected to conductors 35 and 37. Conductors 35 and 36 are separated from conductor 43 by layers 17 and 18 of FIGURE 1e to form another TFT 46, the drain of which is electrically connected to conductor 35, and the source of which is electrically connected to conductor 36. Conductor 40 is electrically connected to conductors 36 and 44, and is separated from conductor 37 by layers 13, 17 and 18 of FIGURE 1e to form a crossover structure 47. The circuit of FIGURE 4 therefore forms a two-transistor inverting circuit, the electrical equivalent of which is illustrated in FIGURE 5. In FIGURE 2 these transistors would be included in drive circuitry 32.

Claims

1. A thin film transistor and crossover structure for a liquid crystal display device, including
 - a transparent electrode layer (12) supported by a transparent substrate (11), said transparent electrode layer being photographically etched and configured into control electrodes (22, 22a), drive lines and data lines (29);
 - a doped layer (13) over selected portions of said transparent electrode layer, forming source (14, 28) and drain (15, 24) regions for said thin film transistor;
 - an undoped layer (17) over said doped layer, forming a channel region (31) between said source (28) and drain (24) regions;
 - a dielectric layer (18) over said undoped layer, forming a gate layer for said thin film transistor;
 - a first conductive layer (19) on selected portions of said dielectric layer (18), making electrical connections to said control electrodes, said drive lines and said data lines; and
 - a second conductive layer (21) on selected portions of said first conductive layer (19), in electrical connection with said first conductive layer (19), said conductive layer having first portions (21a) insulatively spaced from the transparent electrode layer and forming electrode crossovers
- characterized in that said second conductive layer (21) has
 - (i) second portions (21; Figure 1e) extending from respective said drain regions to contact control electrode portions of said transparent electrode layer, and
 - (ii) third portions (21b) connected to said control electrode portions and arranged for connection to external drive circuitry.
2. The structure of claim 1, further characterized by a dielectric coating (33) along the edges of said undoped layer (17) and said dielectric layer (18), for insulating said edges from said second conductive layer (21).
3. The structure of claim 2, characterized in that said first (19) and second (21) conductive layers are of metal.
4. The structure of claim 3, characterized in that said doped layer (13) is of doped amorphous silicon.
5. The structure of claim 4, characterized in that said undoped layer (17) is of undoped amorphous silicon.



tacts the edges of the undoped amorphous silicon layer 17 and the dielectric gate layer 18. This can result in a parasitic resistor between the gate and channel regions of the transistor. The resistance of this resistor can be quite high. However, problems can nevertheless arise under certain circumstances. FIGURE 3 shows a solution to the problem of parasitic resistance. Dielectric stringers 33 are formed over the exposed amorphous silicon edges, to prevent the second metal layer 21 from contacting the edges of the undoped amorphous silicon layer 17. The stringers 33 are formed by depositing a dielectric layer over the entire surface of the device and anisotropically removing the layer from the planar surfaces using a plasma-etch system. The dielectric layer is inherently thicker along the edges of the layers than it is over the planar surface of the layer and, therefore, is not completely removed along the edges during the stripping process. The stringer formation therefore requires only a deposition and an etch step; a photography step utilizing a mask is not required.

FIGURE 4 shows an exemplary drive circuit which can be fabricated along with the TFT's and electrodes of a liquid crystal display device utilizing the claimed method. A plurality of transparent conductors 34, 35, 36 and 37 are formed from the electrode layer 12 of FIGURE 1a. Another plurality of conductors 38, 39, 40 and 41 are formed from the second conductive layer 21 of FIGURE 1e. Another set of conductors 42, 43 and 44 are formed from the first conductive layer 19 of FIGURES 1d and 1e. Conductor 38 is electrically connected to conductors 34 and 42. However, conductors 34 and 35 are partially beneath conductor 42 and are electrically insulated from conductor 42 by layers 17 and 18 of FIGURE 1e to thereby form a TFT 45, the drain of which is electrically connected to conductor 34, and the source of which is electrically connected to conductor 35. Conductor 39 is electrically connected to conductors 35 and 37. Conductors 35 and 36 are separated from conductor 43 by layers 17 and 18 of FIGURE 1e to form another TFT 46, the drain of which is electrically connected to conductor 35, and the source of which is electrically connected to conductor 36. Conductor 40 is electrically connected to conductors 36 and 44, and is separated from conductor 37 by layers 13, 17 and 18 of FIGURE 1e to form a crossover structure 47. The circuit of FIGURE 4 therefore forms a two-transistor inverting circuit, the electrical equivalent of which is illustrated in FIGURE 5. In FIGURE 2 these transistors would be included in drive circuitry 32.

Claims

1. A thin film transistor and crossover structure for a liquid crystal display device, including
 - a transparent electrode layer (12) supported by a transparent substrate (11), said transparent electrode layer being photographically etched and configured into control electrodes (22, 22a), drive lines and data lines (29);
 - a doped layer (13) over selected portions of said transparent electrode layer, forming source (14, 28) and drain (15, 24) regions for said thin film transistor;
 - an undoped layer (17) over said doped layer, forming a channel region (31) between said source (28) and drain (24) regions;
 - a dielectric layer (18) over said undoped layer, forming a gate layer for said thin film transistor;
 - a first conductive layer (19) on selected portions of said dielectric layer (18), making electrical connections to said control electrodes, said drive lines and said data lines; and
 - a second conductive layer (21) on selected portions of said first conductive layer (19), in electrical connection with said first conductive layer (19), said conductive layer having first portions (21a) insulatively spaced from the transparent electrode layer and forming electrode crossovers

characterized in that

said second conductive layer (21) has

 - (i) second portions (21; Figure 1e) extending from respective said drain regions to contact control electrode portions of said transparent electrode layer, and
 - (ii) third portions (21b) connected to said control electrode portions and arranged for connection to external drive circuitry.
2. The structure of claim 1, further characterized by a dielectric coating (33) along the edges of said undoped layer (17) and said dielectric layer (18), for insulating said edges from said second conductive layer (21).
3. The structure of claim 2, characterized in that said first (19) and second (21) conductive layers are of metal.
4. The structure of claim 3, characterized in that said doped layer (13) is of doped amorphous silicon.
5. The structure of claim 4, characterized in that said undoped layer (17) is of undoped amorphous silicon.



6. A method of making a thin film transistor and crossover structure for a liquid crystal display device, including the steps of:

a) applying a transparent conductive electrode layer (12) over one surface of an insulative substrate (11);

b) applying a doped layer (13) over said electrode layer and utilizing a first mask to selectively remove portions of said doped layer and said electrode layer, to form control electrodes, drive lines and data lines from said electrode layer and to form source (14, 28) and drain (15, 24) regions from said doped layer;

c) applying an undoped layer (17) over said pixel electrodes, said lines and said substrate, to form a channel region (31) between said source (28) and drain (24) regions;

d) applying a dielectric layer (18) over said undoped layer;

e) applying a first conductive layer (19) over said dielectric layer and utilizing a second mask, to selectively remove said undoped layer, said dielectric layer and said first conductive layer such that the first conductive layer makes electrical connections to said control electrodes, said drive lines and said data lines; and

f) applying a second conductive layer (21) over said first conductive layer and utilizing a third mask, to selectively remove portions of said second conductive layer, said second conductive layer being formed with first portions (21a) insulatively spaced from the transparent electrode layer and forming electrode crossovers, characterized in that in step f) said second conductive layer (21) is formed with

(i) second portions (21; Figure 1e) extending from respective said drain regions to contact control electrode portions of said transparent electrode layer, and

(ii) third portions (21b) connected to said control electrode portions and arranged for connection to external drive circuitry.

7. The method of claim 6, further characterized by the step of applying an insulative coating over said first conductive layer (19), and of removing said insulative coating from the planar surface of said first conductive layer, to form insulative stringers (33) along the edges of said layers.

8. The method of claim 7, characterized in that said doped layer (13) is of doped amorphous

silicon.

9. The method of claim 8, characterized in that said undoped layer (17) is of undoped amorphous silicon.

10. The method of claim 9, characterized in that said first (19) and second (21) conductive layers are first and second metal layers, respectively.

Patentansprüche

1. Dünnschichttransistor mit Überkreuzungsstruktur für ein Flüssigkristalldisplay, mit

einer transparenten Elektroden-schicht (12), die von einem transparenten Substrat (11) getragen wird und photographisch geätzt und in Steuerelektroden (22,22a), Treiberleitungen und Datenleitungen (29) strukturiert ist,

einer über ausgewählten Teilen der transparenten Elektroden-schicht liegenden dotierten Schicht zur Bildung von Source-(14,28) und Drainzonen (15,24) für den Dünnschichttransistor,

einer auf der dotierten Schicht angeordneten undotierten Schicht (17) zur Bildung einer Kanalzone (31) zwischen der Source- (28) und der Drainzone (24);

einer auf der undotierten Schicht befindlichen dielektrischen Schicht (18) zur Bildung einer Gateelektrode für den Dünnschichttransistor,

einer auf ausgewählten Teilen der dielektrischen Schicht (18) befindlichen ersten leitenden Schicht (19) zur Bildung elektrischer Verbindungen zu den Steuerelektroden, den Treiberleitungen und den Datenleitungen, und

einer auf ausgewählten Teilen der ersten leitenden Schicht (19) befindlichen zweiten leitenden Schicht (21), die mit der ersten leitenden Schicht (19) in elektrischer Verbindung steht und erste Teile (21a) enthält, welche isoliert und im Abstand von der transparenten Elektroden-schicht sind und Elektrodenkreuzungen (30) bilden,

dadurch gekennzeichnet, daß die zweite leitende Schicht (21)

(i) zweite Teile (21; Fig.1e), die sich von jeweils den Drainzonen zur Kontaktierung von Steuerelektrodenzonen der transparenten Elektroden-schicht erstrecken, und

(ii) dritte Teile (21b) aufweist, die mit den Steuerelektrodenzonen verbunden sind und zum Anschluß an eine äußere Treiberschaltung ausgebildet sind.

2. Struktur nach Anspruch 1, weiterhin gekennzeichnet durch einen entlang der Kanten der undotierten Schicht (17) und der dielektrischen



Schicht (18) verlaufenden dielektrischen Überzug (33) zur Isolierung dieser Kanten von der zweiten leitenden Schicht (21).

3. Struktur nach Anspruch 2, dadurch gekennzeichnet, daß die erste und die zweite leitende Schicht (19,21) aus Metall bestehen.

4. Struktur nach Anspruch 3, dadurch gekennzeichnet, daß die dotierte Schicht (13) aus dotiertem amorphem Silizium besteht.

5. Struktur nach Anspruch 4, dadurch gekennzeichnet, daß die undotierte Schicht (17) aus undotiertem amorphem Silizium besteht.

6. Verfahren zur Herstellung eines Dünnschichttransistors und einer Überkreuzungsstruktur für ein Flüssigkristalldisplay, mit den Schritten:

a) Aufbringen einer transparenten leitenden Elektroden Schicht (12) auf einer Oberfläche eines isolierenden Substrates (11),

b) Aufbringen einer dotierten Schicht (13) auf der Elektroden Schicht und Verwendung einer ersten Maske zur selektiven Entfernung von Teilen der dotierten Schicht und der Elektroden Schicht zur Bildung von Steuerelektroden, Treiberleitungen und Datenleitungen aus der Elektroden Schicht und zur Bildung von Source- und Drainzonen (14,28 bzw. 15,24) aus der dotierten Schicht,

c) Aufbringen einer undotierten Schicht (17) auf den Steuerelektroden, den Leitungen und dem Substrat zur Bildung einer Kanalzone (31) zwischen der Source- und der Drainzone (28 bzw. 24),

d) Aufbringen einer dielektrischen Schicht (18) auf der undotierten Schicht,

e) Aufbringen einer ersten leitenden Schicht (19) auf der dielektrischen Schicht und Verwendung einer zweiten Maske zur wahlweisen Entfernung der undotierten Schicht, der dielektrischen Schicht und der ersten leitenden Schicht derart, daß letztere elektrische Verbindungen zu den Steuerelektroden, den Treiberleitungen und den Datenleitungen bildet, und

f) Aufbringen einer zweiten leitenden Schicht (21) auf der ersten leitenden Schicht und Verwendung einer dritten Maske zur wahlweisen Entfernung von Teilen der zweiten leitenden Schicht, welche mit ersten Teilen (21a) gebildet ist, die isoliert und im Abstand von der transparenten Elektroden Schicht sind und Elektrodenüberkreuzungen bilden,

dadurch gekennzeichnet, daß im Schritt f) die zweite leitende Schicht (21) gebildet

wird und mit

(i) zweiten Teilen (21; Fig. 1e), die sich von jeweils den Drainelektroden zur Kontaktierung von Steuerelektrodenzonen der transparenten Elektroden Schicht erstrecken und

(ii) dritten Teilen (21b), die mit den Steuerelektrodenzonen verbunden sind und zum Anschluß an eine externe Treiberschaltung ausgebildet sind.

7. Verfahren nach Anspruch 6, weiterhin gekennzeichnet durch den Schritt des Aufbringens eines isolierenden Überzugs auf der ersten leitenden Schicht (19) und des Entferns des isolierenden Überzugs von der ebenen Oberfläche der ersten leitenden Schicht zur Bildung isolierender Wände (33) entlang den Kanten der Schichten.

8. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß die dotierte Schicht (13) aus dotiertem amorphem Silizium besteht.

9. Verfahren nach Anspruch 8, dadurch gekennzeichnet, daß die undotierte Schicht (17) aus undotiertem amorphem Silizium besteht.

10. Verfahren nach Anspruch 9, dadurch gekennzeichnet, daß die erste und die zweite leitende Schicht (19,21) eine erste bzw. zweite Metallschicht sind.

Revendications

1. Structure de croisement et de transistors à couches minces pour un dispositif d'affichage à cristaux liquides comprenant :

une couche électrode transparente (12) supportée par un substrat transparent (11), ladite couche électrode transparente étant découpée photographiquement et configurée en électrodes de commande (22, 22a), lignes de commande et lignes de données (29) ;

une couche dopée (13) sur des portions sélectionnées de la couche électrode transparente, formant des régions de source (14, 28) et de drain (15, 24) pour ledit transistor à couche mince ;

une source non dopée (17) sur ladite couche dopée, formant une région canal (31) entre lesdites régions de source (28) et de drain (24) ;

une couche diélectrique (18) sur ladite couche non dopée, formant une couche grille pour ledit transistor à couche mince ;

une première couche conductrice (19) sur des portions sélectionnées de ladite couche



diélectrique (18) formant des connexions électriques pour lesdites électrodes de commande, lesdites lignes de commande et lesdites lignes de données ; et

une seconde couche conductrice (21) sur des portions sélectionnées de ladite première couche conductrice (19), en liaison électrique avec ladite première couche conductrice (19), ladite couche conductrice ayant des premières portions (21a) espacées, de façon isolée, de la couche électrode transparente et formant des croisements d'électrodes,

caractérisée en ce que

ladite seconde couche conductrice (21) comporte :

- (i) des secondes portions (21; figure 1e) s'étendant à partir desdites régions de drain respectives pour venir contacter des portions d'électrode de commande de ladite couche électrode transparente, et
- (ii) des troisièmes portions (21b) connectées aux dites portions d'électrode de commande et disposées de manière à assurer la liaison avec le circuit de commande extérieur.

2. Structure selon la revendication 1, caractérisée en outre par un revêtement diélectrique (33) le long des arêtes de ladite couche non dopée (17) et de ladite couche diélectrique (18), pour isoler lesdites arêtes de ladite seconde couche conductrice (21).

3. Structure selon la revendication 2, caractérisée en ce que lesdites première (19) et seconde (21) couches conductrices sont en métal.

4. Structure selon la revendication 3, caractérisée en ce que ladite couche dopée (13) est en silicium amorphe dopé.

5. Structure selon la revendication 4, caractérisée en ce que ladite couche non dopée (17) est en silicium amorphe non dopé.

6. Procédé de fabrication d'une structure de croisement et de transistors à couches minces pour un dispositif d'affichage à cristaux liquides comprenant les étapes consistant à :

a) appliquer une couche électrode conductrice transparente (12) sur une surface d'un substrat isolant (11) ;

b) appliquer une couche dopée (13) sur ladite couche électrode et utiliser un premier masque pour enlever sélectivement des portions de ladite couche dopée et de ladite couche électrode, afin de former des électrodes de commande, des lignes de

commande et des lignes de données à partir de ladite couche électrode et pour former des régions de source (14, 28) et de drain (15, 24) à partir de ladite couche dopée ;

c) appliquer une couche non dopée (17) sur lesdites électrodes pixels, lesdites lignes et ledit substrat, pour former une région canal (31) entre lesdites régions de source (28) et de drain (24) ;

d) appliquer une couche diélectrique (18) sur ladite couche non dopée ;

e) appliquer une première couche conductrice (19) sur ladite couche diélectrique et utiliser un second masque, pour enlever sélectivement ladite couche non dopée, ladite couche diélectrique et ladite première couche conductrice de façon que la première couche conductrice forme des connexions électriques vis-à-vis des électrodes de commande, desdites lignes de commande et desdites lignes de données ;

f) appliquer une seconde couche conductrice (21) sur ladite première couche conductrice et utiliser un troisième masque, pour enlever sélectivement des portions de ladite seconde couche conductrice, ladite seconde couche conductrice étant formée avec des premières portions (21a) espacées de façon isolée de ladite couche électrode transparente et formant des croisements d'électrodes, caractérisé en ce que pendant l'étape f) la seconde couche conductrice (21) est formée avec

(i) des secondes portions (21 ; figure 1e) à partir des régions respectives de drain pour contacter des portions d'électrodes de commande de ladite couche électrode transparente et

(ii) des troisièmes portions (21b) connectées auxdites portions d'électrodes de commande et disposées de manière à assurer la connexion avec le circuit de commande externe.

7. Procédé selon la revendication 6, caractérisé en outre par l'étape qui consiste à appliquer un revêtement isolant sur ladite première couche conductrice (19) et à enlever ledit revêtement isolant de la surface plane de ladite première couche conductrice, afin de former des cordons isolants (33) le long des arêtes desdites couches.

8. Procédé selon la revendication 7, caractérisé en ce que ladite couche dopée (13) est en silicium amorphe dopé.



9. Procédé selon la revendication 8, caractérisé en ce que ladite couche non dopée (17) est en silicium amorphe non dopé.

10. Procédé selon la revendication 9, caractérisé en ce que lesdites première (19) et seconde (21) couches conductrices sont respectivement des première et seconde couches métalliques.

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