The invention proceeds from an evaluation circuit according to the preamble of claim 1.

Such a circuit is known, for example, from DE-A-3 526 051.

For recording digital signals, e.g. CD, R-DAT, DVS, DVT, it is standard practice to record an NRZI signal. In the NRZI signal, the logical one is characterized by a level transition. As a result, the transmitted information is independent of the signal polarity. This is the actual advantage of NRZI recording. With the above-mentioned recording method, so-called m/n modulation is used. Here, one or more n-bit code words are associated with each m-bit data word, with n being greater than m. In the case of CD, 14-bit code words are associated with 8-bit data words. When assembling the coded signal, to comply with the runlength and DC conditions 3 additional bits are in each case inserted between two code words so that, for 8 data bits, there are in each case 17 bits in the coded signal (cf., for example, EP-A-58081).

An m/n code defined by a table has the advantage that error propagation is avoided. Said advantage is retained with CD, although an NRZI signal is recorded since additional bits are disposed between the individual code words. With the other recording methods mentioned, the 8/10 modulation is used without additional bits between the code words. However, when no additional bit is inserted between the code words, the NRZI conversion leads to a signal which is no longer error propagation-free. When, namely, in the reproduced signal the last bit of a code word recorded in NRZI is jammed, upon reconversion of the code words into NRZ the first bit of the next code word is also reversed. With 8/10 modulation, therefore, one false bit in the sampled signal leads to two false bytes in the demodulated signal. With 8/10 modulation, said error propagation occurs in around 10% of all bit errors. For said reason, m/n modulation without NRZI conversion should be employed if no additional bits are used between the code words.

The object of the invention is to avoid error propagation from one code word to the next code word and yet to retain the advantage of polarity independence provided by NRZI conversion.

Said object is achieved by the invention indicated in claim 1. Advantageous developments of the invention and another possible way of achieving said object are indicated in the sub-claims.

The use of synchronizing words with a fixed bit pattern is known (DE-A-3 500 115).

After determination of the signal polarity, it may be ensured by means of an exclusive OR gate that the transmitted signal is always supplied with the correct polarity to the demodulator input.

Another possible way of avoiding polarity dependence of the signal consists of using an m/(n-1) code instead of the m/n code and inserting an additional bit between the code words. Said code may be recorded as an NRZI signal and be demodulated back to NRZ without there being any risk of error propagation.

An embodiment of the invention is described below with reference to the drawings.

Fig. 1 shows, by way of the cutout from an R-DAT data transmission, how one bit error causes two byte errors.

Fig.2 shows a circuit for correcting the polarity of an NRZ signal. The circuit is simultaneously used for synchronizing signal detection.

Fig.3 shows the signal profiles in order to explain the circuit according to Fig.2.

An NRZ signal of indeterminate polarity and the associated bit timing are supplied to the inputs of the circuit according to Fig.2. The NRZ signal contains, in the run-in signal or distributed over the remaining signal, fixed bit patterns SW by which the correct signal polarity may be recognized. Said patterns may be used simultaneously for block synchronization.

In the circuit, the voltage B, whose characteristic is independent of the polarity of the input signal, is first obtained with the aid of the D-type

flipflop 1 and the exclusive OR gate 2. Thus, the bit pattern, which triggers determination of the signal polarity, is recognizable independently thereof. Said pattern SW here comprises 10 bits or, at the output of the gate 2, 9 bits (signal B). The S/P transformer 3 and the comparator 4 are used to recognize the pattern. The output of the comparator changes to high, as soon as the last bit of the pattern B is read into the S/P transformer, for the duration of one bit (signal S). Said time coincides with the last bit of the pattern SW at the output A. The value of said bit is stored in the flipflop 6 (signal C) and, with the aid of the exclusive OR gate 7, adjusts the correct polarity of the NRZ signal.

The signals shown in Fig.3 apply to a case where the input signal already has the correct polarity.

Claims

1. Evaluation circuit for a binary signal in which code signals (SW) are transmitted, which enable determination of the polarity of the binary signal, characterized in that, by evaluating the level transitions, the time position of the code signal (SW) is recognized independently of the polarity of the binary signal and that from said time position is derived the sampling instant of a specific bit of a predetermined value transmitted together with the code signal for establishing the instantaneous signal polarity and its value is determined by sampling.

2. Circuit according to claim 1, characterized in that, by using a time window for the code signal, spurious evaluations caused by bit patterns which simulate the code signal are avoided.

3. Circuit according to claim 1, characterized in that, after adjustment of the correct polarity which is confirmed, for example, by an error detection circuit, the polarity setting is invariable up to a new signal segment.

4. Circuit according to claim 1, 2 or 3, characterized in that the circuit is combined with the circuit for synchronizing signal detection.

5. Circuit according to one or more of claims 1 to 4, characterized in that adjustment of the polarity of the binary signal is effected with the aid of an exclusive OR gate (7).

* C L M S *