17 JUN 2004



# SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING THE SAME

## BACKGROUND OF THE INVENTION

### FIELD OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device, and more particularly to a technique which is effective to prevent a wire from being broken.

### DESCRIPTION OF THE PRIOR ART

In a conventional process of assembling a semiconductor integrated circuit, the following steps have been performed. That is, in an Ag spot plating step, an Ag spot plating is applied to a front end portion (including portions obtained by wire bonding a chip and a lead frame by an Au wire) of a lead of a pressed or etched lead frame (hereinafter, refer to an inner lead) molded by a mold. Next, in a step of assembling a package, a die bonding, a wire bonding and an assembly of the package to be molded are performed. In a thereafter outer plating step (including a dipping step), in order to mount to a printed circuit board or a circuit board, a Sn-Pb system solder layer is previously attached to a portion including a contact portion between a lead which is not molded by the mold (hereinafter, refer to an outer lead) and the substrate in accordance with an outer plating. After the Ag spot

plating step and the outer plating step mentioned above are finished, the step goes to a step of working a product.

However, in recent years when a countermeasure to an environmental problem is required, in particular, as is indicated in Japanese Unexamined Patent Publication No. 5-270860 (USP No. 5,633,090) or the like with respect to Pb, they say that it is required to reduce Pb to a level suitable for the countermeasure against the environmental problem even in a general electronic part such as a semiconductor integrated circuit device or the like and a mounting board.

Conventionally, in order to reduce Pb, the countermeasure is performed by replacing the Sn-Pb solder employed in the outer plating step by the other solder (alloy) containing no Pb as a main metal, that is, a Pb-free alternate solder (a solder composed of a Pb-free metal). The Pb-free alternate solder is required to have a range of melting temperature similar to that of Sn-Pb and an excellent bonding property, particularly a wetting property. No composition completely satisfying the requirements presently exists, and the solders are selectively used in correspondence to the members such as the printed circuit board, the chip part, the semiconductor package and the like. Accordingly, there has been proposed various compositions in a Sn-base alloy based on Sn in

correspondence to various usage, for example, an invention in which Sn-Bi system is employed in place of the Sn-Pb system for the metal employed for the solder layer attached to and formed in the conventional lead, in Japanese Unexamined Patent Publication No. 10-93004 (prior art 1). Further, with respect to a structure of the metal composition of the solder, there is proposed an invention in which the package outer lead and the substrate are mounted by using a Sn-Ag-Bi system solder, in Japanese Unexamined Patent Publication No. 11-179586 (WO 99 30866) (prior art 2).

In the case of employing a Sn-Pb eutectic alternate Pb-free solder for the outer plating, the Sn-base alloy is selected at every usage in the same manner as that mentioned in the prior art, however, in particular, in parts mounted on the vehicle, significantly developed mobile electronic devices and parts with high reliability, an alloy excellent in a bonding strength and a heat resisting fatigue property is desired. There has been known a Sn-Ag system alloy as a Sn-base alloy in the case of attaching great importance to an excellent bonding strength, an excellent heat resisting fatigue property and a high reliability, and a melting point of the Sn-Pb eutectic solder is generally 183°C, on the contrary, a melting point of most of the Sn-Ag system alloy is 200°C or more and is higher than the melting point of the Sn-Pb eutectic solder. Accordingly, it is unavoidable that a

17 JUN 2004



reflow temperature at a time of mounting the semiconductor integrated circuit with using the Sn-Pb eutectic alternate Pb-free solder becomes high in the present. Then, the inventors of the present application mounts the semiconductor integrated circuit device on which the inner lead is Ag-plated and the outer lead is plated by using the Pb-free alternate solder having a melting point higher than that of the Sn-Pb eutectic solder, at a reflow temperature higher than the conventional one and estimates the product. As a result, the inventors ascertain that a product inferiority is generated due to the wire disconnection.

SUMMARY OF THE INVENTION

Accordingly, a purpose of the present invention is to provide means for effectively preventing a wire disconnection generated at a time when a semiconductor integrated circuit device on which an outer lead is plated by using a Pb-free alternate solder having a melting point higher than that of a Sn-Pb eutectic solder is mounted at a reflow temperature higher than the conventional one.

Another purpose of the present invention is to provide means for effectively preventing a wire disconnection generated due to an increase of calorie generally applied to a semiconductor integrated circuit device in addition to an increase of a reflow temperature.

A description will be briefly given of a summary of a representative invention among the inventions disclosed in the present application. Accordingly, there is provided a semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which the connecting member is connected, and an alloy layer having a melting point higher than that of a solder having Pb as a main composition metal and containing no Pb as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin for molding the connected portion.

The invention mentioned above employs Pd as a metal provided through means for attaching and forming the portion to which the connecting member is connected in accordance with a plating or the like. Because there is no problem in a bonding property between a wire such as an Au wire or the like corresponding to the connecting member having a conductivity and a frame material corresponding to the connected material such as a Cu alloy and a 42 alloy, there is a reduced disadvantage generated by a recess of a capillary since Pd is a harder metal in comparison with Ag, and there is a reduced dispersion of thickness of a metal attached to each of the connected members. In this case, a place to be attached and formed is set to the

17 JUN 2004



portion to which the connecting member is connected because the place should be restricted to a minimum area as far as no problem is applied to the bonding property with the connecting member since Pd is not inexpensive with respect to the Sn-Pb system alloy and Ag, and in particular, the cost reduction object can not be effectively achieved in the case of being used for attaching and forming the portion outside the mold body such as the outer lead or the like having a large area.

With respect to the problem such as a plating crack or the like which may be generated due to a molding process or the like of applying a physical deforming force to the attached and formed portion after attaching and forming, the present invention does not have such a problem since the plated portion is molded and is not formed nor worked. Further, there are advantages such that a migration of Ag can be avoided, a virulently poisonous cyanogen is not required at a time of plating and the like.

Further, the connected member is structured such that the alloy having the melting point higher than that of the solder having Pb as the main composing metal and containing no Pb as the main composing metal is attached to and formed in the portion outside the portion molded by the resin, because it is intended that the other materials than a Cu frame such as 42Ni-Fe alloy or the like corresponding to the material of

the frame corresponding to the connected member can be employed, and it is intended to avoid inherent problems to a whole surface Pd plating such that a cost reduction can not be achieved in view of a material cost when applying the same Pd plating as that of the front end portion of the inner lead thereto.

Further, the inventors of the present application have found that the technical idea of the present invention that the Pd plating is applied to the front end portion of the inner lead can be also applied to narrowing the wire together with a chip shrink in view that it is possible to reduce a dispersion of a plating thickness and increase a bonding strength.

Accordingly, a description will be briefly given of a summary of another representative invention among the inventions disclosed in the present application. Accordingly, there is provided a semiconductor integrated circuit device comprising:

a wire having a diameter equal to or less than 30 $\mu$m;

a connected member in which a metal layer including a palladium layer is provided at a portion to which the wire is connected, and a solder containing Pb as a main composition metal is provided at a portion outside a portion molded by a resin; and

a resin for molding the connected portion.

Since the palladium metal layer is attached to and formed on the connecting member, whereby a

bonding strength is improved, the structure is effective to improve an assembly yield and a reliability with respect to an increase of the number of pins and an increase of size in the package, and narrowing of wire (a wire diameter is equal to or less than the present size 30 $\mu$m) caused by the chip shrink, even in the present in which a Pb-free solder is no completely employed. Further, since it is sufficient that the palladium metal layer is attached to and formed on the portion to be connected, the palladium metal layer may be attached to and formed on a tab in addition to the front end portion of the inner lead in accordance with the relation between a cost of the attaching and forming step and a cost of the material.

A description will be in detail given of particulars that the invention described in the present application is considered.

The inventors of the present application have repeatedly estimated so as to find the reason by which the wire is disconnected, and have newly defined the reason of generation. As a result of the inventor's analysis, it has been found that an inferiority of lead side disconnection in the wire is considered to be classified into "an inferiority of wire disconnection after molding" and "an inferiority of lead adhered portion disconnection after reflowing". At first, it is considered that the inferiority of wire disconnection after molding is caused by a stress

generated due to a vibration of the lead and a stress generated due to a resin hardening and shrinking. As shown in Fig. 1, when charging the resin from a gate 33 (a charging time is 10 seconds), a front end potion of an inner lead 4 is vertically vibrated due to a resin stream. A stress is applied to a wire 19 due to the vibration, and particularly, the vibration stress tends to be applied to a pin near the gate portion. Further, since the resin is hardened and shrunk from a position apart from the gate 33 toward the gate 33 (from right to left in the drawing), it is considered that a tensional force is applied to the wire 19 and the wire disconnection is generated from the lead side adhered portion having a relatively weak bonding strength.

Next, it is considered that the inferiority of lead adhered portion disconnection after reflowing is generated due to difference between an expansion 36 of the lead frame and an expansion 35 of the resin. Fig. 2 is a schematic view explaining the matter mentioned above. Physical properties of the resin hardened material are largely changed at a glass transition point Tg (150 to 160°C) of the resin, and particularly, a coefficient of thermal expansion $\alpha$ (= 1.4) in an area ($\alpha 2$) equal to or more than Tg becomes about four to five times a value in an area ($\alpha 1$) equal to or less than Tg. Since the temperature at a time of reflowing is higher than the temperature of Tg, a damage is applied to the wire 19 due to the resin

expansion ($\alpha 2$) at a time of reflowing, a crack 37 is generated at a portion having a small strength (an A portion in Fig. 2), and the disconnection is generated due to a difference 34 between the expansion 36 of the lead frame and the expansion 35 of the resin, as shown in Fig. 3.

Since the reflow temperature is increased by using the alternate solder made of the Sn-base alloy having a high melting point for the reason of employing the Pb-free solder, the calorie applied to the package is increased, and in particular, the difference between the expansion of the lead frame and the expansion of the resin is promoted. Accordingly, it has been found that the inferiority of disconnection in the lead side adhered portion after reflowing particularly becomes a problem among the inferiority of wire disconnection mentioned above.

In this case, the inventors of the present application have estimated a relation between a thickness of the Ag plating and the wire disconnection. As a result, it has been clarified that the wire disconnection is easily generated when the thickness of plating becomes a predetermined thickness range. Analyzing the reason thereof, it can be considered that an area of connecting surface between Ag and Au can not be sufficiently secured at a time of adhering the Au wire in a too thin plating thickness, whereby the wire disconnection is generated in accordance with a wire

deformation due to a thermal stress. Further, when making the Ag plating thicker than a certain thickness, the Ag plating surface is deformed at a degree equal to or more than necessity so as to absorb a bonding energy. As a result, it is considered that it is impossible to obtain a sufficient bonding, and a cross sectional shape of the bonding surface becomes formed in a shape being weak with respect to a tension against the thermal deformation of the Au wire.

Further, a description will be given of an inferiority of disconnection in the lead side adhered portion after reflowing in view of a shape. Fig. 4 is a cross sectional view when the wire 19 is adhered to the Ag spot plating surface by a capillary 20. A hatched portion in Fig. 4 corresponds to a front end of the capillary 20, a diameter of the front end is 170 $\mu$m, and a diameter of the Au wire 19 is 30 $\mu$m. In the drawing, a thickness of the lead frame 7 is 150 $\mu$m. As mentioned above, since the thickness of the Ag plating 38 is dispersed in a range between about 1.5 $\mu$m and 10 $\mu$m at each of the lead frames to be Ag-plated, it is hard to define the thickness of the Ag plating. Accordingly, in the drawing, it is supposed that the plating thickness at which the inferiority of disconnection is considered to be generated is comparatively thick.

In the case of adhering the wire, since Ag is a relatively soft metal, the capillary 20 sinks into

the surface of the Ag plating 38, and a part of the surface of the Ag plating 38 rises up as shown in Fig. 4. Then, the thickness of the Au wire 19 in a portion denoted by reference symbol A in Fig. 4 becomes relatively thin, whereby a portion having a weakened wire strength is generated. Fig. 5 is a perspective view of the lead side adhered portion after bonding. In Fig. 5, a portion denoted by a line A in Fig. 5 corresponds to the A portion in Fig. 4. After reflowing, the wire disconnection is generated from the A portion in Fig. 4 as shown in Fig. 6 due to the difference between the expansion of the lead frame and the expansion of the resin. For reference, Fig. 7 is a perspective view of the lead side adhered portion of the inferiority of wire disconnection after molding. The inferiority of disconnection in the lead side adhered portion after reflowing is generated so that the disconnected wire overlaps with the adhered portion, however, the inferiority of wire disconnection in the lead side adhered portion after molding is generated so that the disconnected wire is apart from the adhered portion. As mentioned above, it is apparent on the basis of the analysis of the inventors of the present application that the wire disconnection is generated by the reason that the capillary 20 sinks into the surface of the Ag plating having a comparatively large thickness so as to generate the portion having the weakened wire strength.

In recent years, the thickness of the Ag plating required on design has become thin to some μm. As a result of estimating the dispersion of the thickness of the surface of the Ag plating, it has been known that in the current Ag plating process, it is hard to maintain an initial set plating thickness at a time of treating a lot of subjects to be plated, and the plating thickness is dispersed in a range between 1.5 μm and 10 μm at each of the subjects to be plated. Accordingly, the inventors of the present application have tried so that the maximum thickness is within a range between 5 and 8 μm rather than the conventional 10 μm, in order to restrict the dispersion of the thickness of the Ag plating at each of the lead frames. However, in the current Ag plating process, the maximum thickness 10 μm is a limit as mentioned above, and it has been hard to set the maximum thickness in the range between 5 and 8 μm. Accordingly, it is considered that it is hard in the current Ag plating process to make the dispersion of the plating thickness smaller than the current level.

Then, in order to solve the problems mentioned above that the portion having the weakened wire strength is generated, the present invention can be achieved by considering a new idea of using a metal being harder than Ag and having a little dispersion of thickness for the metal layer attached to and formed in the front end portion of the inner lead, and estimating

and considering so as to employ an appropriate metal for making a production cost minimum.

Next, a description will be given of a reason that the palladium metal layer is attached to and formed in the front end portion of the inner lead as mentioned above, whereby the disconnection of the lead side adhered portion after reflowing can be prevented, in view of the shape of the lead side adhered portion.

Fig. 8 is a cross sectional view when the wire 19 is adhered to the surface of the Pd plating 10 by the capillary 20. There is described an embodiment in which a hatched portion in Fig. 8 is a front end of the capillary 20, a diameter of the front end is 170 $\mu$m, and a diameter of the Au wire 19 is 30 $\mu$m. In the case of adhering the wire 19, since Pd is a relatively hard metal, the capillary 20 does not sink so much in comparison with the case that the plating surface is Ag. Accordingly, a thickness t of the Au wire 19 in a portion A in Fig. 8 can be secured to a sufficient thickness in comparison with the portion A in Fig. 4, so that it is possible to keep the wire strength. Fig. 9 is a perspective view of the lead side adhered portion after bonding. A portion denoted by a line A in Fig. 9 corresponds to the portion A in Fig. 8. It is known that the thickness of the Au wire in Fig. 9 can be secured in comparison with that in Fig. 5. After reflowing, the stress is applied in a direction of an arrow in Fig. 9 due to the difference between the

expansion of the lead frame and the expansion of the resin. However, since there is no portion having a weakened strength, the disconnection so that the disconnected wire overlaps with the adhered portion which is generated at the Ag plating is not generated. The wire disconnection is not at least generated when the adhering force of the capillary 20 is set so as to secure 10 $\mu$m or more of the thickness t of the Au wire when the thickness of the lead frame 7 is 150 $\mu$m, the thickness of the Pd plating 10 is 0.02 $\mu$m at the minimum and 0.15 $\mu$m at the maximum.

Next, a description will be given of a reason why the technical idea of the present invention for attaching and forming the Pd metal layer to the member to be connected can be applied to a technique of narrowing the connecting member without relation to the Pb-free.

As a result of estimating the conditions in the representative invention in accordance with the present application, an attention is paid to the fact that an estimation is performed on the assumption that a size of the package is not changed. In this case, the wire disconnection is caused by the difference between the expansion of the lead frame and the expansion of the resin as mentioned above. Accordingly, it is considered that the difference of the expansion mentioned above becomes further significant when the package is enlarged in accordance

with the multi pins. Since the capacity is increased, the calorie becomes large, so that the calorie applied to the resin at a time of reflowing is increased. Further, due to the multi pins, the calorie flowing from the substrate through the pin at a time of reflowing is also increased.

Further, even in the case that the pitch is narrowed due to the chip shrink, a lot of calorie is applied to the package in comparison with the package having the same size. Accordingly, the package size becomes small due to the chip shrink even in the package having the same number of pins, the pad pitch of the wire bonding is narrowed in accordance therewith, and the wire diameter becomes small. In accordance with narrowing of the wire caused by the chip shrink, that is, in accordance that the current wire diameter 30 $\mu$m becomes further narrow, it is considered that there is generated a necessity of making the plating thickness thin. Because it is considered that the dispersion of the plating thickness within the range capable of being realized in the current Ag spot plating process is too large in the future and the bonding operation becomes unstable.

That is, the matter that the calorie applied to the package is increased due to the narrow pitch in accordance with the multi chips and the chip shrink even when the reflow temperature is not changed corresponds to the matter that the reflow temperature

is increased. Accordingly, the technical idea of attaching and forming the Pd metal layer to the member to be connected can be applied in view that it is possible to reduce the dispersion of the metal thickness and increase the bonding strength, without direct relation to the Pb-free.

In this case, although the technical idea is different from the invention described in the present application at all, there is a pre-solder plated lead frame(PPL) process as a treating method in which the Pb-free can be realized. The PPL process is a process for plating on a whole of the lead frame including the die bonding portion, the inner lead and the outer lead before molding with using the palladium metal having a good bonding property. The PPL process can be made Pb-free since the metal used in the plating is palladium. Further, in the PPL process, since an outer plating process conventionally performed after molding is not required, it is possible to shorten an assembling time and automate a whole of the assembling process due to omission of a solder plating in the outer lead.

However, since a local battery is formed in accordance with a potential difference between a material of the frame member and Pd material, there is a risk that a corrosion is generated, so that an Fe system frame such as 42 alloy (42Ni-Fe) metal or the like can not be used as the frame member, and the frame is limited to a copper alloy. In this case, the Fe

system frame can be used by inserting a barrier metal between the frame and the Pd metal layer, however, since a material in the cross section is exposed at a time of cutting the dam bar and the front end of the lead in an actual assembly process, and a material corrosion is concentrically accelerated from the cross section, and since this Fe system frame becomes disadvantageous in view of the manufacturing cost due to complexity of the manufacturing process, so that this structure is not proper. Further, since the plating of the outer lead is applied from the frame state, the outer lead surface is contaminated and the solder wetting property at a time of mounting the substrate is deteriorated in a burr removing operation for removing resin burrs or the like generated by molding at a high possibility. Further, since the palladium is a hard metal in comparison with the lead system solder, there is generated a problem that a plating is peeled if the outer lead is formed after plating.

Accordingly, even if the Pd plating process mentioned above is employed as means for achieving the object of the present invention, that is, preventing the wire disconnection, it is basically possible to make the difference of the plating thickness at each of the subjects to be plated small, however, since there are the disadvantages mentioned above, it is a matter of course that the means is improper to the solving

means for the problems.

Further, the inventors of the present application have searched known arts before filing the present application in view of "plating Pd on the lead frame". As a result, in Japanese Unexamined Patent Publication Nos. 11-40723 (U.S.P. No. 5,889,317) (a known art 3) and 11-220084 (a known art 4), there is proposed an invention that a part or a whole of a lead including at least an outer lead is plated by a Pd system metal. Further, as an invention that a whole of a lead is plated by a Pd system metal mainly in view of requiring no outer plating process and automating a whole of an assembly process, there have been proposed Japanese Unexamined Patent Publication Nos. 10-284666 (a prior art 5), 10-298798 (a prior art 6) and 10-18056 (a prior art 7), and in view of further applying an Au-Ag alloy plating onto an outermost surface of a Pd system metal layer, there is proposed Japanese Unexamined Patent Publication No. 11-8341 (a prior art 8).

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view showing a mechanism by which an inferiority of wire connection is generated after molding;

Fig. 2 is a schematic view showing a mechanism by which a crack is generated in a lead side adhered portion after reflowing;

Fig. 3 is a schematic view showing a wire disconnection generated in a lead side adhered portion after reflowing;

Fig. 4 is an enlarged view of a wire bonding onto a surface of an Ag plating at a time of adhering a wire;

Fig. 5 is a perspective view of a wire adhered portion of the wire bonding onto the surface of the Ag plating;

Fig. 6 is a schematic view showing a wire disconnection after reflowing the Ag plating;

Fig. 7 is a schematic view showing a wire disconnection after a resin of the Ag plating is hardened and shrunk;

Fig. 8 is an enlarged view of a wire bonding onto a surface of a Pd plating at a time of adhering a wire;

Fig. 9 is a perspective view of a wire adhered portion of the wire bonding onto the surface of the Pd plating;

Fig. 10 is a plan view of a lead frame corresponding to one embodiment in accordance with the present invention;

Fig. 11 is an enlarged plan view of a lead frame corresponding to one embodiment in accordance with the present invention;

Fig. 12 is a cross sectional view along a line A-B in Fig. 11;

Fig. 13 is a cross sectional view showing details of a Pd plating in a front end of an inner lead;

Fig. 14 is a schematic view showing an adhesive material application in a die bonding process using a frame in accordance with the present invention;

Fig. 15 is a schematic view showing a chip mounting in the die bonding process using the frame in accordance with the present invention;

Fig. 16 is a schematic view showing a wire bonding process using the frame in accordance with the present invention;

Fig. 17 is an enlarged view showing a Pd plating portion in the die bonding process using the frame in accordance with the present invention;

Fig. 18 is a schematic view showing a shape of an Au wire adhered portion at a time of wire bonding onto the surface of the Pd plating;

Fig. 19 is a perspective view of the adhered portion of the wire bonding onto the surface of the Pd plating;

Fig. 20 is an enlarged plan view of a lead frame corresponding to one embodiment in accordance with the present invention after the wire bonding is completed;

Fig. 21 is a cross sectional view of a resin molding process using the frame in accordance with the present invention;

Fig. 22 is a cross sectional view after plating an outer lead using the frame in accordance with the present invention;

Fig. 23 is a schematic view showing a bending process using the frame in accordance with the present invention;

Fig. 24 is a schematic view showing a lead front end aligning process using the frame in accordance with the present invention;

Fig. 25 is a top elevational view of a completed product of a package using the frame in accordance with the present invention;

Fig. 26 is a cross sectional view along a line E-F of the completed product of the package using the frame in accordance with the present invention;

Fig. 27 is a perspective view of the completed product of the package using the frame in accordance with the present invention;

Fig. 28 is a schematic view showing a structure in which the package in accordance with the present invention is mounted on a substrate;

Fig. 29 is a top elevational view of the mounting substrate after the package in accordance with the present invention is mounted; and

Fig. 30 is a schematic cross sectional view of a Fan-In type CSP of a peripheral pad structure.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

A description will be in detail given below of an embodiment in accordance with the present invention with reference to the accompanying drawings. In this case, the same reference numerals are attached to elements having the same functions in all the drawings for explaining the embodiment, and an overlapping description will be omitted.

A semiconductor integrated circuit device in accordance with the present embodiment is a semiconductor integrated circuit device in which a front end portion of an inner lead is palladium spot plated and an outer lead is Sn-Ag system alloy plated.

In the present embodiment, there is exemplified a structure having 208 pins and a package size of 28 mm square.

Four repeated units of a lead frame used in the semiconductor integrated circuit device are described in Fig. 10. It is a matter of course that the number of the repeated units is not limited to four. Further, a material is a Cu alloy in the present embodiment, however, may be an iron system lead frame such as 42Ni-Fe or the like. In the present embodiment, since the palladium plating is not applied to a whole surface, the local battery in the outer lead which is a problem in the palladium whole surface plating is not generated.

Fig. 11 is an enlarged view of one lead frame 7 in which a palladium plating 1 is applied to a front

end portion of the inner lead 4. A tab (die pad) 2 is a so-called small tab, and an area of a chip mounting surface is set to be smaller than an area of a main surface of a semiconductor chip mounted thereon. By using the small tab, it is possible to previously prevent a risk that a reflow crack is generated. In accordance with the present embodiment, the tab is a small tab, however, may be a cross tab type (a type having only a width of a suspending lead 3), and may be also a normal tab. Further, in accordance with the present embodiment, no palladium plating is applied to the die pad 2, however, a palladium plating may be applied to the die pad 2.

Fig. 12 is a cross sectional view along a line A-B of the enlarged view of the lead frame 7 shown in Fig. 11. The palladium plating 1 is applied to the front end portion of the lead. A portion to be palladium plated may be structured such that the wire bonding portion has a size to be spot plated at the minimum. At a time of plating, the plating is performed by masking the other portions than the back surface of the lead frame 7 and the front end portion of the lead in accordance with an electrolytic plating. Accordingly, the plating is applied in a thickness direction in addition to the plating on the surface of the front end of the inner lead necessary at the minimum mentioned below. A description will be exemplified of the case the wire bonding is performed

with respect to the plating area necessary at the minimum by using the Au wire 19 having the wire diameter of 30 μm, a minimum necessary area 21 of the spot plating is about 75 % of an area a x b of the wire adhered portion expressed by an adhered width a and an adhered length b, as shown in Fig. 19. In accordance with the present embodiment, both of the values a and b are set to be at least 90 μm, and a position of the minimum necessary area 21 is set so that a center thereof is arranged at 300 μm from the front end of the lead frame.

Further, a so-called tab descent for positioning the die pad 2 below the surface of the inner lead 4 by deforming the suspending lead 3 is performed. This is because a difference of resin charging speed between upper and lower portions of the chip is reduced at a time of charging the resin, whereby a vibration can be prevented.

Fig. 13 shows a structure of a palladium plating in the front end portion of the inner lead in accordance with the present embodiment. The palladium plating is constituted by three layers, and is structured such that a Ni plating 11 is at first applied to the inner lead 4 as a ground plating, a palladium plating 10 is applied thereon and an Au flash plating 9 is finally applied in order to improve a corrosion resistance. Particular thickness of the respective layers in accordance with the present

17 JUN 2004



embodiment are set such that a thickness of the inner lead is 150 μm, a thickness of the Ni plating is 1.0 μm, a thickness of the palladium plating is 0.15 μm and a thickness of the Au flash plating is about 1 nm.

A description will be given of the die bonding process with reference to Fig. 14. Fig. 14 is a cross sectional view along a line C-D in Fig. 11. The lead frame 7 after descending the tab is mounted on a stage 16 and is brought into contact with a lower surface of the die pad 2. An adhesive material 15 for die bonding is adhered on an upper surface of the die pad by positioning a dispenser 13 having a syringe 12 receiving the adhesive material 15 above the die pad. In this case, the adhesive material 15 employs a conductive paste (an organic resin containing Ag powders and carbons) for a semiconductor device having a small consumed power. Characteristics required for the die bonding material are a solder wetting property with respect to a coated film of the semiconductor device and the lead frame 7, a thermal fatigue property of a solder due to a temperature difference between a semiconductor device used time and a semiconductor device unused time and the like in addition to a good heat transmitting property. The conductive paste is effective in the view mentioned above. Further, since the object of the present invention is to reduce Pb, a metal solder mainly composed of Pb which is generally used in a power device is not used. However, this does

not mean that no metal solder is used, and a Pb-free solder can be used. In this, in the case of another representative invention taking the Pb-free into no consideration, it is a matter of course that a metal solder mainly composed of Pb may be employed. The next step will be described with reference to Fig. 15. After moving a semiconductor chip 18 above the lead frame to which the adhesive material 15 is adhered by a collet 17, the chip is adhered to a chip adhering position. A cross sectional shape of the collet 17 is formed in a quadrangular pyramid as shown in Fig. 15, and the collet 17 and the semiconductor chip 18 are closely attached to the collet 17 in accordance with a vacuum suction.

A description will be given of the wire bonding process with reference to Fig. 16. After the die bonding process, a lower surface of the chip 18 and a lower surface of the inner lead 4 are fixed to the stage 16. A portion in which the die pad 2 such as a notch or the like is received is previously provided in the stage 16. After fixing, the capillary 20 is bonded onto the inner lead 4 from the pad on the chip 18. Fig. 17 is an enlarged view of a wire bonding portion. Fig. 18 is a schematic view of a shape of the adhered portion after wire bonding. In the case of the present invention, the wire diameter d is 30 $\mu$m, the adhered width W is 105 $\mu$m at the maximum, and the adhered length is 105 $\mu$m at the maximum. It is apparent from

17 JUN 2004



the result of estimation performed by the inventors that a good adhered state can be obtained by setting a relation among L, W and d so as to satisfy the formulas $1.5 \leqq W/d \leqq 3.5$ and $1.5 \leqq L/d \leqq 3.5$.

The lead frame 7 obtained after the wire bonding process mentioned above is completed is as shown in Fig. 20, and a resin molding is next performed in the molding process. In the molding process, the lead frame 7 is held between molding metal molds 22, and a resin 24 is poured from a resin charging port 23. In the present embodiment, a time for pouring is structured such that a charging time becomes 10 seconds. At a time of pouring, it is necessary that the resin is poured at the same speed between the upper and lower portions of the lead frame 2. This is because an vibrating width of the lead frame 7 is set to be as small as possible at a time of molding and a stress applied to the wire 19 is reduced so as to prevent the wire from being disconnected.

Fig. 22 shows a state in which the outer plating is applied to the outer lead 5 after molding the resin, and the outer plating is completed. The metal used for the outer plating in the present embodiment is an alloy obtained by adding Cu and/or Bi to the Sn-Ag system metal. This is because Pb reduction is realized and a reflow mounting having a high reflow temperature is supposed. Accordingly, it is a matter of course that it is possible to employ an

alloy among Zn, In, Sb and Sn or an Sn system alloy in addition to the alloy mentioned above. In the case of the reflow mounting, a bonding cream solder includes a structure having a different mounting temperature such as an Sn-Ag system, an Sn-Zn system, an Sn-Bi system and the like. In the current state, the Sn-Ag system metal has a melting point higher than a melting point of the Pb containing solder. However, in the other embodiment, the outer plating uses a lead system solder. This is because in the case of paying attention to the fact that the bonding strength between the inner lead 4 and the wire 19 is increased by applying the palladium plating to the inner lead 4, it is not necessary to limit the outer plating to the lead system solder.

After the outer plating is completed, there is a process of forming the outer lead 5. At first, as shown in Fig. 23, the resin molding body is held and fixed at a root portion of the outer lead 5 and the outer lead 5 is formed by a punch 25. After forming, the front end portion of the outer lead 5 is cut and formed by moving a die 26 from a lower portion as shown in Fig. 24.

Fig. 25 is a schematic view of a completed product in the present embodiment, Fig. 27 is a perspective view of the schematic view and Fig. 26 is a cross sectional view along a line E-F in Fig. 27. The number of pins is 208, however, the reduced number of

17 JUN 2004



pins are illustrated in the drawings in order to avoid troublesome. The shape of the resin molding body is obtained by beveling one corner and cutting a sign so as to secure a directivity of the package at a time of handling for mounting. In particular sizes of the completed product in the present embodiment, a size D of the resin molding body is 28 mm square, an outer size of the semiconductor package including the outer lead 5 is 30.6 ± 0.2 mm, and a height is 3.56 mm at the maximum. Further, a pitch p of the lead is 0.5 mm, a width w of each of the leads is 0.2 mm, and a thickness t is 0.15 mm. A length a in a horizontal direction between the resin molding body and the front end of the outer lead is 1.3 mm, and a length k of the front end of the bent outer lead is 0.5 mm.

A description will be given of a process of mounting on a printed circuit board with reference to Figs. 28 and 29. A solder paste 28 is applied onto a foot print 29 greater than the mounting surface in the front end of the outer lead 5. The mounting operation is performed by arranging a package 31 from the above after application and applying a heat. The reflowing methods include a vapor phase reflow, an air reflow, an infrared rays reflow and the like. In the embodiment, the reflow temperature is 255°C , and is 20°C higher than the reflow temperature 235°C of the normal Sn-Pb system solder. This is because it is possible to correspond to the fact that the melting point of the

solder is high. Further, in the particular sizes of the foot print 29 on the printed circuit board 30, a width a is 0.20 to 0.25 mm and a length b is 1.3 mm.

This is because within the range of the size, a little shift of the position of the package generated at arranging it can be self-aligned by the reflow, so that there is not generated a problem caused by the shift of the mounting position.

In the embodiment mentioned above, the description is given of the case that the present invention is employed for the purpose of manufacturing QFP, however, the present invention can be applied to a surface mounting type package such as QFN, QFJ or the like without being limited to QFP, and further the present invention can be applied to general packages having wire connecting portions such as a small outline non-leaded package in which a pad arranged in the middle of a chip is connected to a lead by a wire. Further, in accordance with the embodiment, the structure is made such as to improve a connecting strength of the portion in which the wire corresponding to the connecting member is adhered and connected to the inner lead corresponding to the member to be connected, however, the connecting member is not limited to the wire, and the member to be connected is not limited to the lead. For example, the present invention can be applied to the case of applying the Pd plating to a pad 40 corresponding to a portion for

adhering and connecting a lead corresponding to a connecting member 42 to a semiconductor chip 39 in a chip size package or the like which employs an insulative member such as a polyimide tape 43 or the like for a base material and is mounted on a substrate by a solder ball as shown in a schematic cross sectional view in Fig. 30. That is, the present invention can be generally applied to improvement of connecting property and reliability in the connecting portion, in the semiconductor device.

A description will be briefly given of effects obtained by the representative invention among the inventions disclosed by the present application.

In accordance with the present invention, it is possible to provide an LSI package corresponding to the lead-free, in particular, an LSI package using the lead-free alternate solder having a melting point higher than that of the Pb system solder, and it is possible to improve an assembling yield and a reliability. Further, it is possible to provide an LSI package corresponding to the narrow wire caused by the increase of pins in the package or the increase of size thereof and the chip shrink, and it is possible to improve an assembling yield and a reliability.

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected;

a resin molding said portion to be connected; and

a member electrically connected to said connected member in which an alloy layer having a melting point higher than that of a solder having Pb as a main composition metal and containing no Pb as a main composing metal is provided at a portion outside said resin.

2. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and an alloy layer having a melting point higher than that of a solder having Pb as a main composition metal and containing no Pb as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin molding said connected portion.

3. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a metal layer having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pb and Pd as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin molding said connected portion.

4. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a Pb-free metal layer having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pd as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin molding said connected portion.

5. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a connecting member connected to said semiconductor chip and having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a Pb-

free metal layer having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pd as a main composing metal is provided in the other portions;

a resin molding a portion of said semiconductor chip connected to said connecting portion, said connecting member and a portion of said connected portion to which said connecting member is connected.

6. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a wire bonded to said semiconductor chip;

a lead in which a metal layer including a palladium layer is plated on a portion in an inner lead bonded by said wire, a Pb-free alternate solder having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pd as a main composing metal is plated on a mounted portion of an outer lead;

a resin molding a bonding portion of said semiconductor chip to which said wire is bonded, said wire and the inner lead of said lead including a portion to which said wire is bonded.

7. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a wire;

a resin molding said semiconductor chip and

17 JUN 2004



said wire; and

a lead in which a metal layer including a palladium layer is provided in a front end of a portion molded by said resin, and a Pb-free metal layer having a melting point higher than an Sn-Pb eutectic solder and containing no Pd as a main composing metal is provided in a portion outside a portion molded by said resin.

8. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a lead in which a front end portion of an inner lead is plated by Pd and an outer lead is plated by a Pb-free solder;

a wire bonding said semiconductor chip and the inner lead of said lead; and

a resin molding said semiconductor chip, the inner lead portion of said lead and said wire,

wherein a melting point of said Pb-free alternate solder is higher than a melting point of an Sn-Pb eutectic solder, and said Pb-free alternate solder is not composed of only Pd.

9. A mounting substrate comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to

which said connecting member is connected, and an alloy containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board,

wherein said semiconductor integrated circuit device is connected to said printed circuit board by a solder having a melting point higher than that of the solder having Pb as a main composing metal.

10. A mounting substrate comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a metal containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board to which said semiconductor integrated circuit device is connected by a metal having a melting point higher than that of the solder having Pb as a main composing metal.

11. A method of manufacturing a mounting substrate, said mounting substrate comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a

17 JUN 2004



conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and an alloy layer containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board,

wherein said method has a process at which a temperature of said connected member becomes higher than a melting point of an Sn-Pb eutectic solder.

12. A method of manufacturing a mounting substrate, said mounting substrate comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and an alloy layer containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board,

wherein said semiconductor integrated circuit device and said printed circuit board are received within the same furnace and a temperature within said furnace becomes higher than a melting point of an Sn-Pb eutectic solder.

13. A method of manufacturing a mounting

17 JUN 2004



substrate, said mounting substrate comprising:

a semiconductor integrated circuit device provided with a semiconductor chip, a lead in which a Pd metal is plated on a front end portion of an inner lead and a Pb-free metal is plated on an outer lead, a wire bonding said semiconductor chip and said lead, and a resin molding a wire bonding portion of said semiconductor chip, a wire bonding portion of said lead and said wire, wherein a melting point of said Pb-free alternate solder is higher than a melting point of an Sn-Pb eutectic solder, and said Pb-free alternate solder is not composed of only Pd; and

a printed circuit board,

wherein said semiconductor integrated circuit device and said printed circuit board are received in a reflow furnace, and a set temperature of the reflow furnace is higher than a set temperature at a time of reflow mounting the semiconductor integrated circuit device in which a Pb metal layer is provided in an outer lead, to the substrate.

14. A semiconductor integrated circuit device comprising:

a wire having a diameter equal to or less than 30 $\mu$m;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said wire is connected, and a solder containing Pb as a main composition metal is provided at a portion

outside a portion molded by a resin; and

a resin for molding said connected portion.

15. A mounting substrate comprising:

a semiconductor integrated circuit device provided with a semiconductor chip, a lead in which a Pd metal is attached and formed onto a front end portion of an inner lead and a Pb solder layer is attached and formed onto an outer lead, a wire bonding said semiconductor chip and said lead and having a diameter of 30 $\mu$m or less, and a resin molding a wire bonding portion of said semiconductor chip, a wire bonding portion of said lead and said wire; and

a printed circuit board.

16. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer is provided in a portion to which said connecting member is adhered; and

a resin molding said adhered portion,

wherein a thickness of the adhered portion in said connecting member is equal to or more than 10 $\mu$m.

17. A method of manufacturing a plurality of semiconductor integrated circuit devices, said semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a resin; and

a connected member in which a first metal

17 JUN 2004



layer is provided in a portion to which said connecting member is connected, and a second metal layer different from said first metal layer is provided outside a portion molded by said resin, and a resin molding said portion to be connected,

wherein there is provided a process of attaching and forming a metal layer having a difference between a thickness of the first metal layer of a first semiconductor integrated circuit device and a thickness of the first metal layer of a second semiconductor integrated circuit device is less than 10 $\mu$m.