TIME-BASED ACCESS OF A MEMORY CELL

CROSS REFERENCES

[0001] The present Application for Patent claims priority to U.S. Patent Application No. 15/619,163 by Di Vincenzo, entitled "Time-Based Access of a Memory Cell," filed June 9, 2017, which is related to co-pending U.S. Patent Application Number 15/619,158 by Di Vincenzo, entitled "Time-Based Access of a Memory Cell," filed June 9, 2017, each of which is assigned to the assignee hereof, and each of which is expressly incorporated by reference herein.

BACKGROUND

[0002] The following relates generally to time-based access of a memory cell and more specifically to time-based sensing of a logic state of the memory cell.

[0003] Memory devices are widely used to store information in various electronic devices such as computers, wireless communication devices, cameras, digital displays, and the like. Information is stored by programing different states of a memory device. For example, binary devices have two states, often denoted by a logic "1" or a logic "0." In other systems, more than two states may be stored. To access the stored information, a component of the electronic device may read, or sense, the stored state in the memory device. To store information, a component of the electronic device may write, or program, the state in the memory device.

[0004] Various types of memory devices exist, including magnetic hard disks, random access memory (RAM), read only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, phase change memory (PCM), and others. Memory devices may be volatile or non-volatile. Non-volatile memory, *e.g.*, FeRAM, may maintain their stored logic state for extended periods of time even in the absence of an external power source. Volatile memory devices, *e.g.*, DRAM, may lose their stored state over time unless they are periodically refreshed by an external power source. FeRAM may use similar device architectures as volatile memory but may have non-volatile properties due to the use of a ferroelectric capacitor as a storage device. FeRAM devices may thus have improved performance compared to other non-volatile and volatile memory devices.

memory cell. In some examples of the memory array 1005 described above, the current may be forced based at least in part on performing a read operation on the ferroelectric memory cell.

[0161] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for charging, by a current generator, the digit line to the first voltage level based at least in part on applying the current. In some examples of the memory array 1005 described above, the current may be forced by a current generator coupled to the digit line and the node.

[0162] The memory array 1005 may include means for applying a time-varying signal to a latch after initiating a read operation on a memory cell, means for activating the latch based at least in part on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation, and means for identifying a logic state of the memory cell based at least in part on a value of the time-varying signal present at the latch when the latch is activated.

[0163] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for isolating the memory cell from the latch after the digit line charges to the first voltage level as part of the read operation.

[0164] In some examples of the memory array 1005 described above, the memory cell may be configured to store at least three logic states. In some examples of the memory array 1005 described above, the identified logic state of the memory cell may be selected from the at least three logic states.

[0165] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a second time-varying signal to a second latch based at least in part on performing the read operation on the memory cell, the second time-varying signal different from the time-varying signal, the second latch different from the latch.

[0166] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating the second latch based at least in part on the digit line that may be coupled to the memory cell charging to the first voltage level, wherein identifying the logic state of the memory cell may be based at least in part on the

operations of block 1315 may be performed by a logic determiner as described with reference to FIGs. 10 through 12.

[0205] In some cases, a value of the time-varying signal varies in a predetermined manner over a predetermined interval of the time-varying signal. In some cases, the memory cell is configured to store at least three logic states. In some cases, the identified logic state of the memory cell is selected from the at least three logic states. In some cases, a configuration of the second time-varying signal is based at least in part on a configuration of the time-varying signal, wherein the time-varying signal and the second time-varying signal cooperate to define at least three logic states. In some cases, a configuration of the time-varying signal is based at least in part on an expected charge of the memory cell and the first voltage level. In some cases, the configuration of the time-varying signal is based at least in part on a number of logic states the memory cell is capable of storing. In some cases, the configuration of the time-varying signal is based at least in part on a number of latches used in the read operation. In some cases, a configuration of the time-varying signal and an interval of the time-varying signal is predetermined.

[0206] An apparatus for performing the method 1300 is described. The apparatus may include means for applying a time-varying signal to a latch after initiating a read operation on a memory cell, means for activating the latch based at least in part on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation, and means for identifying a logic state of the memory cell based at least in part on a value of the time-varying signal present at the latch when the latch is activated.

[0207] In examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for isolating the memory cell from the latch after the digit line charges to the first voltage level as part of the read operation. In some examples of the method 1300 and apparatus described above, the memory cell is configured to store at least three logic states and the identified logic state of the memory cell is selected from the at least three logic states.

[0208] In some examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for applying a second time-varying signal to a second latch based at least in part on performing the read operation on the memory cell, the second time-varying signal different from the time-varying signal, the second latch different from the latch. Some examples of the method 1300 and apparatus described above

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a memory cell in electronic communication with a digit line;

a sense component coupled to the memory cell, the sense component configured to output a signal that is based at least in part on a duration of time for a voltage level input into the sense component to satisfy a voltage threshold; and

a first latch coupled to the sense component, the first latch configured to output a value of a first signal indicative of a logic state of the memory cell based at least in part on the signal received from the sense component.

2. The apparatus of claim 1, further comprising:

a controller to identify the logic state of the memory cell based at least in part on the value of the first signal when the voltage level input into the sense component satisfies the voltage threshold.

3. The apparatus of claim 1, wherein:

the memory cell is configured to store at least three logic states.

4. The apparatus of claim 3, further comprising:

a second latch coupled to the sense component, the second latch configured to receive a second signal indicative of a first bit of a logic state identifier associated with the memory cell, wherein the first signal is indicative of a second bit of the logic state identifier.

5. The apparatus of claim 4, further comprising:

a controller to identify the logic state of the memory cell based at least in part on the first bit and the second bit of the logic state identifier.

6. The apparatus of claim 1, further comprising:

a cascode having a first node coupled to the digit line and a second node coupled to the sense component, the cascode being configured to apply a voltage to the digit line during a read operation.

7. The apparatus of claim 1, wherein the memory cell comprises:

a ferroelectric capacitor configured to store a polarization state and a dielectric charge state.

8. The apparatus of claim 1, wherein:
the sense component in an inverter.

9. The apparatus of claim 1, wherein:
the first latch is activated by the signal output from the sense component.

10. A method, comprising:
applying a time-varying signal to a latch after initiating a read operation on a memory cell;
activating the latch based at least in part on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation; and
identifying a logic state of the memory cell based at least in part on a value of the time-varying signal present at the latch when the latch is activated.

11. The method of claim 10, further comprising:
isolating the memory cell from the latch after the digit line charges to the first voltage level as part of the read operation.

12. The method of claim 10, wherein:
the memory cell is configured to store at least three logic states; and
the identified logic state of the memory cell is selected from the at least three logic states.

13. The method of claim 12, further comprising:
applying a second time-varying signal to a second latch based at least in part on performing the read operation on the memory cell, the second time-varying signal different from the time-varying signal, the second latch different from the latch.

14. The method of claim 13, further comprising:
activating the second latch based at least in part on the digit line that is coupled to the memory cell charging to the first voltage level, wherein identifying the logic state of the memory cell is based at least in part on the time-varying signal present at the latch

and the second time-varying signal present at the second latch when the latch and the second latch are activated.

15. The method of claim 13, wherein:

a configuration of the second time-varying signal is based at least in part on a configuration of the time-varying signal, wherein the time-varying signal and the second time-varying signal cooperate to define at least three logic states.

16. The method of claim 10, further comprising:

charging the digit line of the memory cell as part of the read operation, wherein the time-varying signal is applied when charging the digit line begins.

17. The method of claim 10, further comprising:

sensing a second voltage level at a node different from the digit line, wherein the latch is activated based at least in part on the second voltage level satisfying a voltage threshold.

18. The method of claim 17, further comprising:

outputting a signal based at least in part on the second voltage level satisfying the voltage threshold, wherein the latch is activated based at least in part on the signal.

19. The method of claim 10, further comprising:

determining that a duration of the read operation satisfies a time threshold, wherein identifying the logic state of the memory cell is based at least in part on the latch not activating prior to the duration satisfying the time threshold.

20. The method of claim 10, wherein:

a configuration of the time-varying signal is based at least in part on an expected charge of the memory cell and the first voltage level.

21. The method of claim 20, wherein:

the configuration of the time-varying signal is based at least in part on a number of logic states the memory cell is capable of storing.

22. The method of claim 21, wherein:

the configuration of the time-varying signal is based at least in part on a number of latches used in the read operation.

23. The method of claim 10, wherein:

the value of the time-varying signal varies in a predetermined manner over a predetermined interval of the time-varying signal.

24. An apparatus, comprising:

a ferroelectric memory cell comprising:

a selection component in electronic communication with an access line;

a ferroelectric capacitor coupled to the selection component, the ferroelectric capacitor configured to store a polarization state and a charge state; and

a controller operable to identify a logic state of the ferroelectric memory cell from a set of at least three logic states based at least in on the polarization state and the charge state.

25. The apparatus of claim 24, further comprising:

a sense component coupled to the ferroelectric memory cell, the sense component configured to output a signal based at least in part on a voltage satisfying a voltage threshold.

26. The apparatus of claim 24, further comprising:

at least two latches coupled to the ferroelectric memory cell, the at least two latches configured to output a value of a first time-varying signal and a value of a second time-varying signal based at least in part on receiving a signal indicative that a voltage satisfies a voltage threshold.

27. The apparatus of claim 24, further comprising:

a cascode coupled to a digit line, the cascode configured to apply a first voltage to the digit line during an access operation.

28. The apparatus of claim 27, further comprising:

a sense component coupled to a node of the cascode different from the digit line, the sense component configured to detect a second voltage present on the node, wherein the second voltage is based at least in part on a voltage level of the digit line.

29. The apparatus of claim 28, further comprising:

a first latch coupled to an output of the sense component, the first latch configured to receive a signal indicative that the second voltage present on the node satisfies a voltage threshold.

30. The apparatus of claim 29, further comprising:

a second latch coupled to the output of the sense component, the second latch configured to receive the signal.

31. The apparatus of claim 30, wherein:

the controller is coupled to outputs of the first latch and the second latch; and

the controller is operable to identify the logic state of the ferroelectric memory cell based at least in part a first output signal received from the first latch and a second output signal received from the second latch.

32. The apparatus of claim 30, wherein:

the first latch is configured to receive a first time-varying signal to indicate at least in part the logic state of the ferroelectric memory cell; and

the second latch is configured to receive a second time-varying signal to indicate at least in part the logic state of the ferroelectric memory cell, the second time-varying signal different from the first time-varying signal.

33. The apparatus of claim 32, wherein:

the first latch is configured to output a value of the first time-varying signal based at least in part on receiving the signal indicative of the second voltage satisfying the voltage threshold; and

the second latch is configured to output a value of the second time-varying signal based at least in part on receiving the signal indicative of the second voltage satisfying the voltage threshold.

34. The apparatus of claim 24, wherein:

the access line is a plate line or a digit line.

35. The apparatus of claim 24, wherein:

the ferroelectric capacitor is coupled to a second access line different from the access line.

36. The apparatus of claim 24, wherein:
the polarization state stored on the ferroelectric capacitor is in a stable state.

37. The apparatus of claim 24, wherein:
the charge state stored on the ferroelectric capacitor is in a volatile state.

38. A method, comprising:
sensing a first state of a ferroelectric capacitor in a ferroelectric memory cell;
sensing a second state of the ferroelectric capacitor different from the first state; and
identifying a logic state of the ferroelectric memory cell from at least three logic states based at least in part on the first state and the second state.

39. The method of claim 38, wherein:
the first state of the ferroelectric capacitor is associated with a polarization of the ferroelectric capacitor.

40. The method of claim 38, wherein:
the second state of the ferroelectric capacitor is associated with a dielectric charge stored on the ferroelectric capacitor.

41. The method of claim 38, further comprising:
identifying a first bit of the logic state based at least in part on the first state; and
identifying a second bit of the logic state based at least in part on the second state.

42. The method of claim 38, further comprising:
activating at least two latches based at least in part on a voltage level of a node different from a digit line satisfying a voltage threshold.

43. The method of claim 42, further comprising:
applying a first time-varying signal to one of the at least two latches; and
applying a second time-varying signal different from the first time-varying signal to another of the at least two latches,

wherein the logic state is identifying based at least in part on values of the first time-varying signal and the second time-varying signal when activating the at least two latches.

44. The method of claim 38, further comprising:

identifying a duration for a first voltage level of a digit line to satisfy a voltage threshold during an access operation, the duration based at least in part on the first state of the ferroelectric capacitor, the second state of the ferroelectric capacitor, and a voltage applied to the digit line.

45. The method of claim 38, further comprising:

identifying a duration for a second voltage level of a node different from a digit line to satisfy a voltage threshold, the duration based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor.

46. A method, comprising:

activating a selection component of a ferroelectric memory cell;

modifying a first state of a ferroelectric capacitor of the ferroelectric memory cell based at least in part on a voltage being applied to the ferroelectric memory cell while the selection component is activated;

deactivating the selection component; and

modifying a second state of the ferroelectric capacitor based at least in part on the selection component being deactivated while the voltage is applied to the ferroelectric memory cell.

47. The method of claim 46, further comprising:

activating the selection component while a plate line and a digit line coupled to the ferroelectric memory cell are grounded or virtually grounded.

48. The method of claim 46, wherein modifying the first state of the ferroelectric capacitor comprises:

applying a first voltage to the ferroelectric capacitor.

49. The method of claim 48, wherein applying the first voltage to the ferroelectric capacitor comprises:

applying a second voltage to a digit line coupled to the ferroelectric memory cell; and

applying a third voltage to a plate line coupled to the ferroelectric memory cell, the third voltage different from the second voltage, wherein the first voltage is based at least in part on the second voltage and the third voltage.

50. The method of claim 46, wherein modifying the second state of the ferroelectric capacitor comprises:

applying a fourth voltage to the ferroelectric capacitor.

51. The method of claim 50, wherein applying the fourth voltage to the ferroelectric capacitor comprises:

applying a fifth voltage to a digit line coupled to the ferroelectric memory cell, the selection component being deactivated while the fifth voltage is applied to the ferroelectric memory cell, wherein the selection component is positioned between the ferroelectric capacitor and a plate line coupled to the ferroelectric memory cell.

52. The method of claim 50, wherein applying the fourth voltage to the ferroelectric capacitor comprises:

applying a sixth voltage to a plate line coupled to the ferroelectric memory cell, the selection component being deactivated while the sixth voltage is applied to the ferroelectric memory cell, wherein the selection component is positioned between the ferroelectric capacitor and a digit line coupled to the ferroelectric memory cell.

53. The method of claim 46, wherein:

the ferroelectric memory cell is configured to store at least three logic states based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor.

54. The method of claim 46, wherein:

the first state is a polarization state of the ferroelectric capacitor; and

the second state is a dielectric charge state of the ferroelectric capacitor.